CIRCUIT DESCRIPTION

U508: Digital filter (SM5814AS)

Introduction:

The SM5814AS is a digital filter LSI for digital audios, developed uniquely by NPC making use of molybdenum-gate CMOS technology. This LSI, a single-chip device, provides quadruple-oversampling output for both channels and is capable of digital attenuation on 6-bit data.

This LSI is a smaller-sized 24-pin SOP realized through employment of serial I/O format.

Features:

Structure

- Molybdenum-gate CMOS

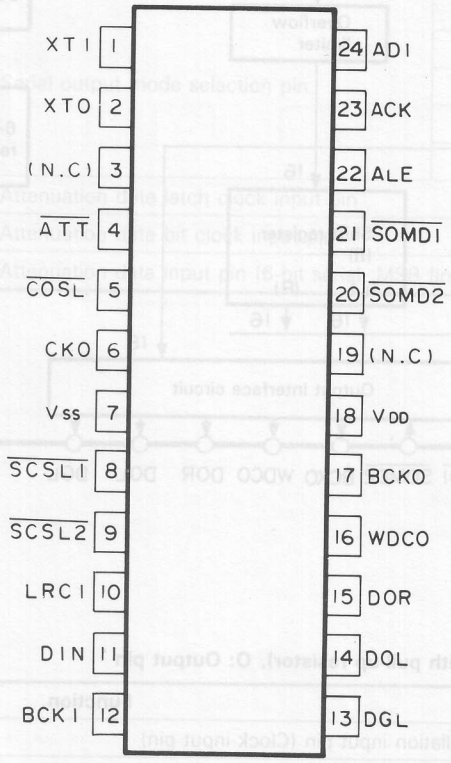
Functions

- Quadruple oversampling for both right and left channels (Input rate fs—output rate 4fs)
- Digital attenuation
- Built-in overflow limiter
- 16-bit 2-DACs/16-bit 1-DAC/I2S/18-bit output mode selection
- 16-bit serial data input/output (2's complement, MSB first)
- Built-in crystal oscillation circuit
- Clock output (2-divided XTI and undivided output selectable)
- Compatible with any of system clocks 384fs, 392fs, 192fs and 256fs
  (However, in the I2S output mode, 392fs is unusable.)

Configuration

- Linear-phase FIR filter n 2 stages (105-order + 21-order)
- Reduced rounding error through employment of 18-bit filter coefficient
- Highly accurate operation by 16 × 18-bit multiplier and 25-bit accumulator
- 64-step digital attenuation

Pin configuration



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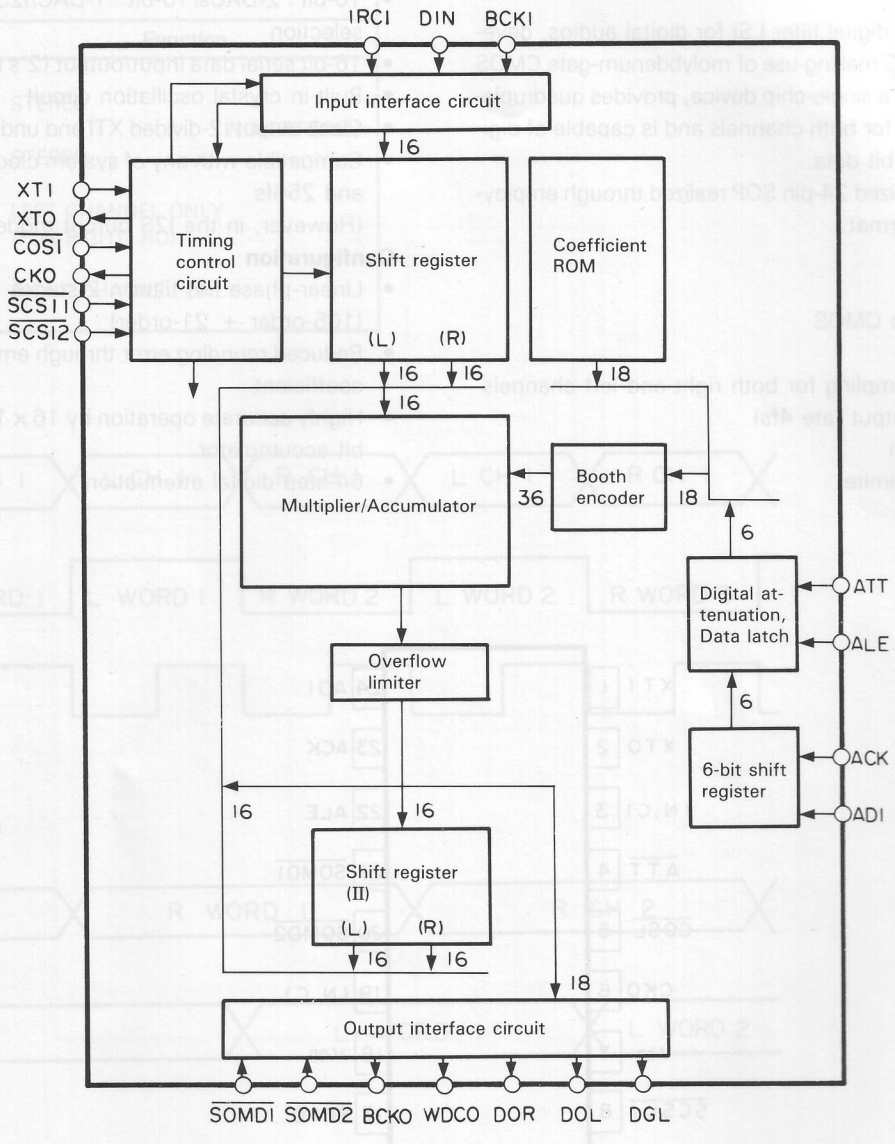
Block diagram



Pin Functions: **Note: I: Input pin (Ip: input pin with pull-up resistor), O: Output pin**

Pin No.	Pin Name	I/O	Function
1	XTI	I	Crystal oscillation input pin (Clock input pin)
2	XTO	O	Crystal oscillation output pin
3		/	(N·C)
4	$\overline{ATT}$	Ip	Digital attenuation O/OFF selection pin $\overline{ATT}$ = "H": Digital attenuation OFF $\overline{ATT}$ = "L" : Digital attenuation ON
5	$\overline{COSL}$	Ip	CKO output selection pin
6	CKO	O	Clock output pin $\overline{COSL}$ = "H": XTI input clock 2-divided output $\overline{COSL}$ = "L": XTI input clock undivided output
7	Vss	/	GND pin

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Pin No.	Pin Name	I/O	Function			
8	$\overline{\text{SCSL 1}}$	Ip	Input clock selection pin	$\overline{\text{SOSL 1}}$	$\overline{\text{SOSL 2}}$	XTI clock
				H	H	384 fs
9	$\overline{\text{SCSL 2}}$	Ip		H	L	392 fs
				L	H	192 fs
				L	L	256 fs
10	LRCI	Ip	Basic sampling rate (fs) sync clock input pin L-ch/R-ch→LRCI = "H"/"L"			
11	DIN	Ip	16-bit serial data input pin (2's complement, MSB first)			
12	BCKI	Ip	Input data bit clock input pin			
13	DGL	O	L-ch output data deglitch signal output pin			
14	DOL	O	$\overline{\text{SOMD 1}}$ = "H", $\overline{\text{SOMD 2}}$ = "H": L-ch data output Others: L-ch/R-ch data reciprocal output			
15	DOR	O	$\overline{\text{SOMD 1}}$ = "H", $\overline{\text{SOMD 2}}$ = "H": Rc-h data output Others: R-ch output data deglitch signal output			
16	WDCO	O	Output data word clock output pin			
17	BCKO	O	Output data bit clock output pin			
18	V_{DD}	/	Supply voltage pin (4.5 ~ 5.5 V)			
19		/	(N·C)			
20	$\overline{\text{SOMD 2}}$	Ip	Serial output mode selection pin	$\overline{\text{SOMD 1}}$	$\overline{\text{SOMD 2}}$	Output mode
				H	H	16-bit 2 DACs
21	$\overline{\text{SOMD 1}}$	Ip		H	L	16-bit 1 DAC
				L	H	I^2S
				L	L	18-bit
22	ALE	Ip	Attenuation data latch clock input pin			
23	ACK	Ip	Attenuation data bit clock input pin			
24	ADI	Ip	Attenuation data input pin (6-bit serial, MSB first)			

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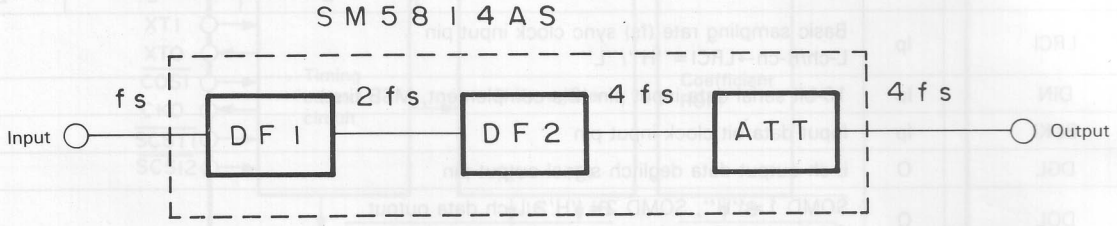
Function Description

Quadruple Oversampling:

In this LSI, the L-ch/R-ch data entered at sampling rate fs is output at sampling rate 4fs through the quadruple oversampling by digital filtering.

This LSI realizes the quadruple oversampling by the cascade connection of linear-phase FIR filters in two stages.



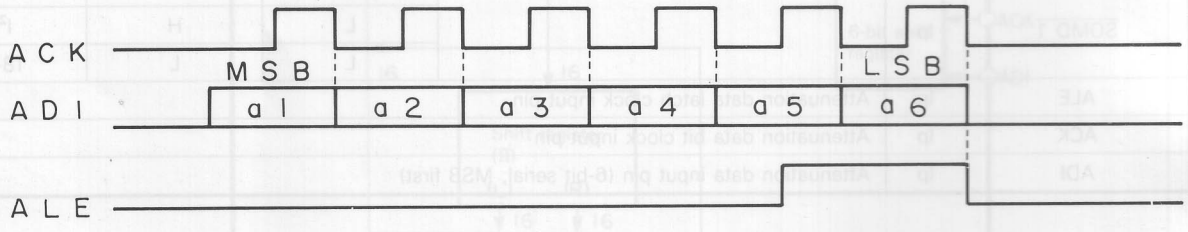
DF1, DF2: Linear-phase FIR twice oversampling digital filters
ATT: Digital attenuation

Digital Attenuation:

In this LSI, the digital attenuation turns ON by making the $\overline{ATT}$ pin "L".

The attenuation level is set by the 6-bit data (attenuation data) input to the ADI, ACK and ALE pins.

It is necessary that the data input to the ADI pin be represented as no-code absolute values of MSB first 6-bit serial data and be varying in synchronization with the trailing edge of the ACK.



The setting of the attenuation data on the above timing can be performed asynchronously with the digital filtering.

In addition, when the $\overline{ATT}$ pin is made "H" (or open), the attenuation data is reset and the digital attenuation goes OFF.

The digital attenuation operation is performed by multiplying the digital-filtered data by the coefficient based upon the attenuation data.

This coefficient is generated as follows:

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Digital Attenuation Coefficient (18-bit)

a) Code bit

b)
Bitwise inversion of
attenuation data

c)
Low-order 11 bits are
all "1".

The relationship between the attenuation data and the attenuation level in this digital attenuation operation is as follows:

Attenuation data						Attenuation level
a1	a2	a3	a4	a5	a6	
0	0	0	0	0	0	0 dB
0	0	0	0	0	1	−0.137 dB
0	0	0	0	1	1	−0.276 dB
0	1	1	1	1	1	−5.735 dB
1	0	0	0	0	0	−6.021 dB
1	0	0	0	0	1	−6.296 dB
1	1	1	1	1	0	−30.103 dB
1	1	1	1	1	1	−36.124 dB

Level [dB] = 20 × log (64-DATA)/64)
Level: Attenuation level
Data: Attenuation data

Serial Input:

(1) Correspondence between LRCI polarity and data

In this LSI, the discrimination between L-ch and R-ch is made by the LRCI polarity to take data in. The correspondence between the LRCI polarity and the data is as follows:

L-ch/R-ch → LRCI "H"/"L"

Clock:

(1) Clock input selection

The system clock of this LSI is a crystal oscillator or an external clock input to the XTI pin. Which clock frequency is input to the XTI pin is determined depending upon the states of the $\overline{\text{SCSL 1}}$ and $\overline{\text{SCSL 2}}$ pins.

Condition		Clock input to XTI pin
$\overline{\text{SCSL 1}}$	$\overline{\text{SCSL 2}}$	
H	H	384 fs
H	L	392 fs
L	H	192 fs
L	L	256 fs

fs: Input sampling rate
Note: When the I^2S mode is engaged, 392fs is unusable as the system clock.

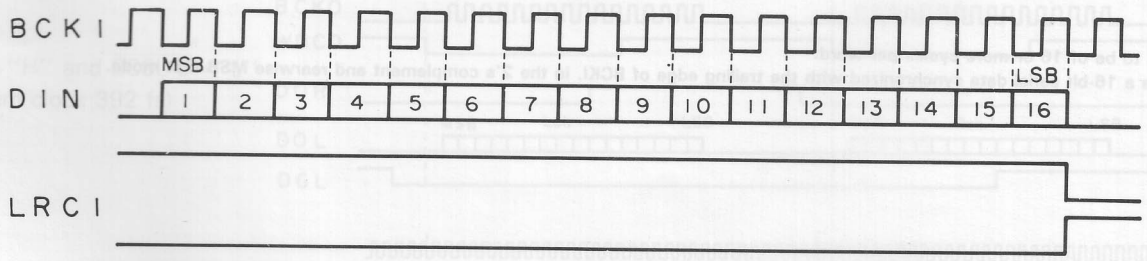
(2) Clock output selection

In this LSI, from the its CKO pin, a clock is output for the signal processing LSI, etc. Using this clock output, it is easier to realize a system for which one crystal oscillation is used as the master clock.
Which clock frequency is output from the $\overline{\text{CKO}}$ pin is determined depending upon the state of the COSL pin as follows:

$\overline{\text{COSL}}$ = "H" (or open): 2-divided output of XTI input clock
$\overline{\text{COSL}}$ = "L" : Undivided output of XTI input clock

(2) Serial data input

In this LSI, the 16-bit serial data is taken into a 16-bit shift register at the leading edge of BCKI, in the 2's complement and MSB first mode. Then, the data is latched into the data latch by the level change of LRCI at 16 bits/word separately for L-ch and R-ch. At this time, the discrimination between L-ch and R-ch is performed by the level of LRCI.



CIRCUIT DESCRIPTION

Serial Output:

In this LSI, four serial output modes are available, from which one is selected according to the states of the $\overline{\text{SOMD 1}}$ and $\overline{\text{SOMD 2}}$ pins.

Condition		Serial output mode
$\overline{\text{SOMD 1}}$	$\overline{\text{SOMD 2}}$	
H	H	(I) 16-bit 2-DAC
H	L	(II) 16-bit 1-DAC
L	H	(III) I^2S
L	L	(IV) 18-bit

(I) 16-bit 2-DAC mode

$\overline{\text{SOMD 1}}$ = "H" (or open), $\overline{\text{SOMD 2}}$ = "H" (or open)

This mode is for L-ch/R-ch in-phase conversion using two 16-bit D/AC converters.

(II) 16-bit 1-DAC mode

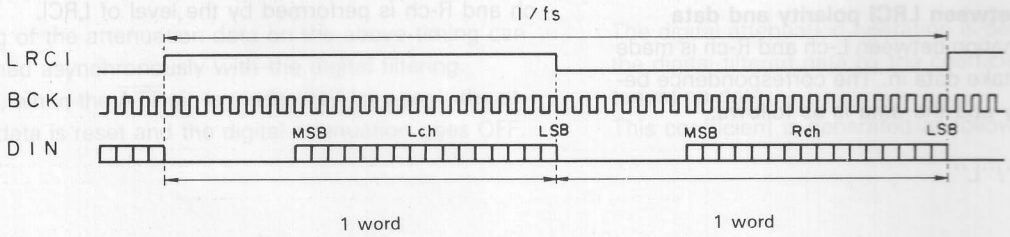
$\overline{\text{SOMD 1}}$ = "H" (or open), $\overline{\text{SOMD 2}}$ = "L"

This mode is for D/A conversion using one 16-bit D/A converter and separation between L-ch and R-ch by the sample-hold circuitry.

When this mode is engaged, DGL is used for the switching signal of the L-ch sample-hold circuit and DOR is for the switching signal of the R-ch sample-hold circuit.

Timing Diagram:

Serial Input Timing



- **BCKI needs to be of 16 or more cycles per word.**
- **DIN shall be a 16-bit serial data synchronized with the trailing edge of BCKI, in the 2's complement and rearwise MSB first mode.**

(III) I^2S mode

$\overline{\text{SOMD 1}}$ = "L", $\overline{\text{SOMD 2}}$ = "H" (or open)

(IV) 16-bit mode

$\overline{\text{SOMD 1}}$ = "L", $\overline{\text{SOMD 2}}$ = "L"

This mode performs serial data output in a 18-bit form, and is used when a digital attenuator is used, thereby suppressing the reduction in dynamic range due to the digital attenuation.

*** For the serial output timing and format, refer to the timing chart.**

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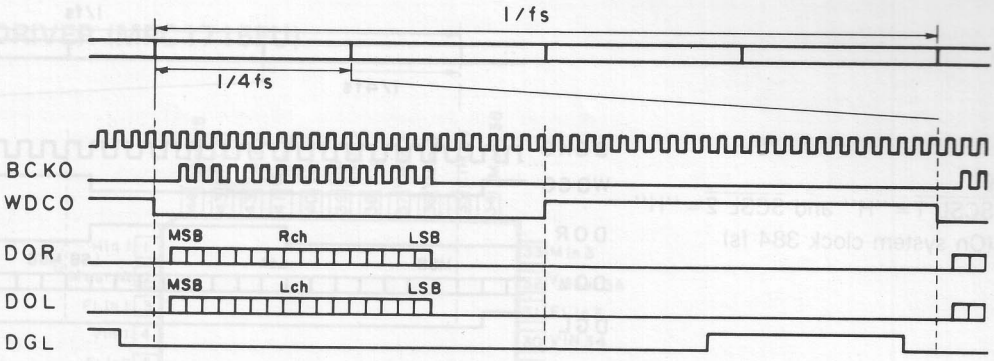
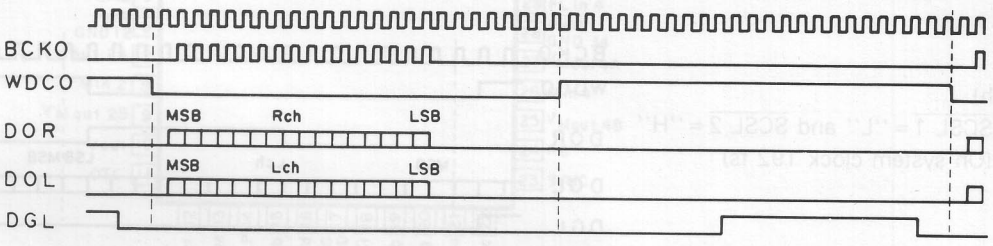
Serial Output Timing

(1) 16-bit 2-DAC mode: $\overline{\text{SOMD 1}}$ = "H" (or open), $\overline{\text{SOMD 2}}$ = "H" (or open)

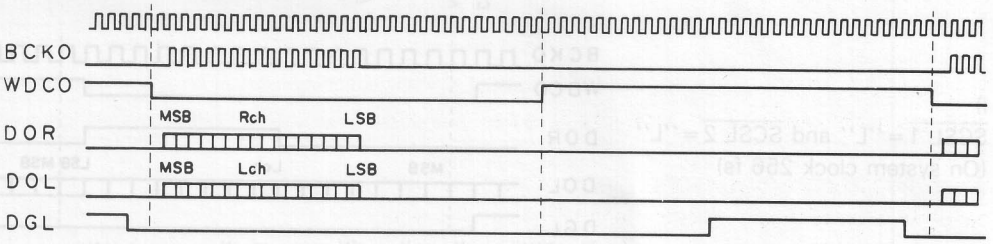
a)
$\overline{\text{SCSL 1}}$ = "H" and $\overline{\text{SCSL 2}}$ = "H"
or
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "H"
(On system clock 384fs or 192 fs)



b)
$\overline{\text{SCSL 1}}$ = "H" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 392fs)

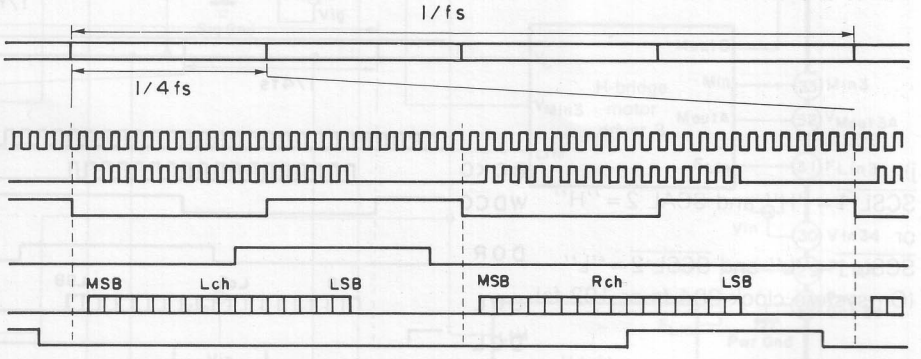


c)
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 256 fs)

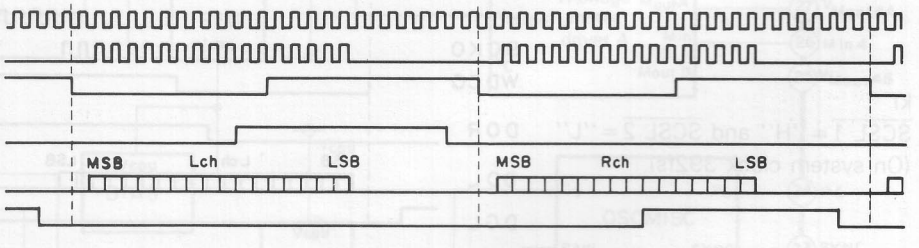


(2) 16-bit 1-DAC mode: $\overline{\text{SOMD 1}}$ = "H" (or open) and $\overline{\text{SOMD 2}}$ = "L"

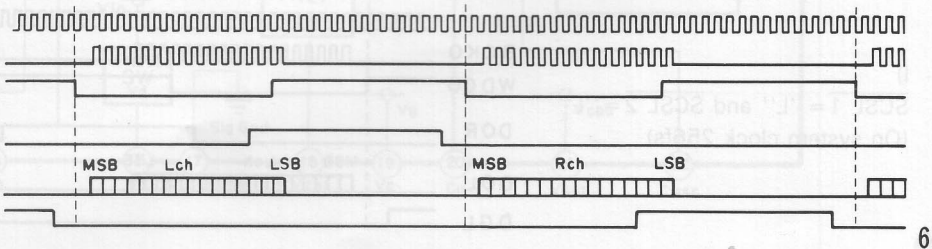
d)
$\overline{\text{SCSL 1}}$ = "H" and $\overline{\text{SCSL 2}}$ = "H"
or
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "H"
(On system clock 384fs or 192 fs)



e)
$\overline{\text{SCSL 1}}$ = "H" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 392 fs)



f)
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 256 fs)



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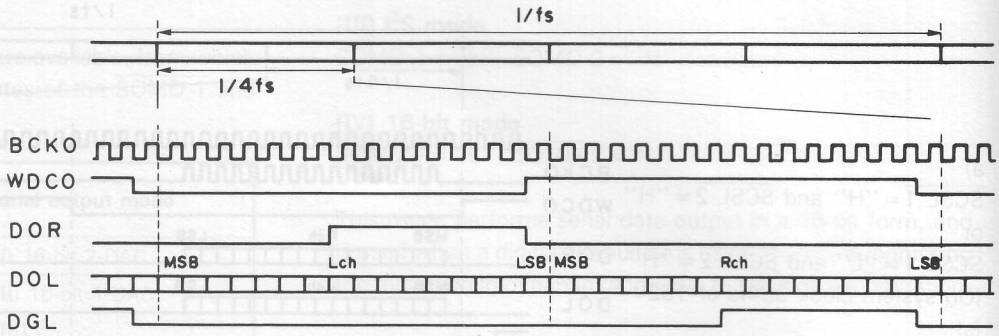
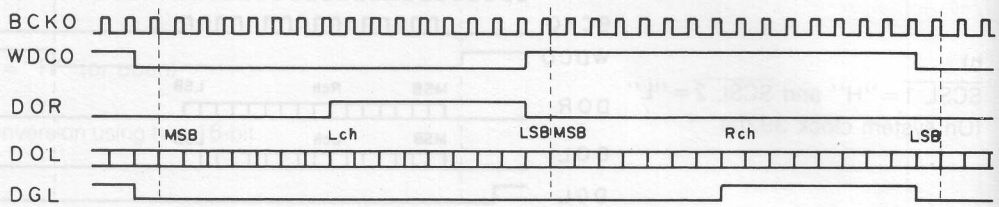
(3) I²S mode: $\overline{\text{SOMD 1}}$ = "L" and $\overline{\text{SOMD 2}}$ = "H" (or open)

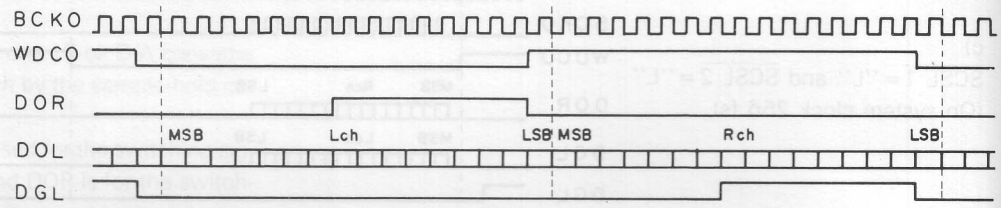
g)
$\overline{\text{SCSL 1}}$ = "H" and $\overline{\text{SCSL 2}}$ = "H"
(On system clock 384 fs)



h)
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "H"
(On system clock 192 fs)

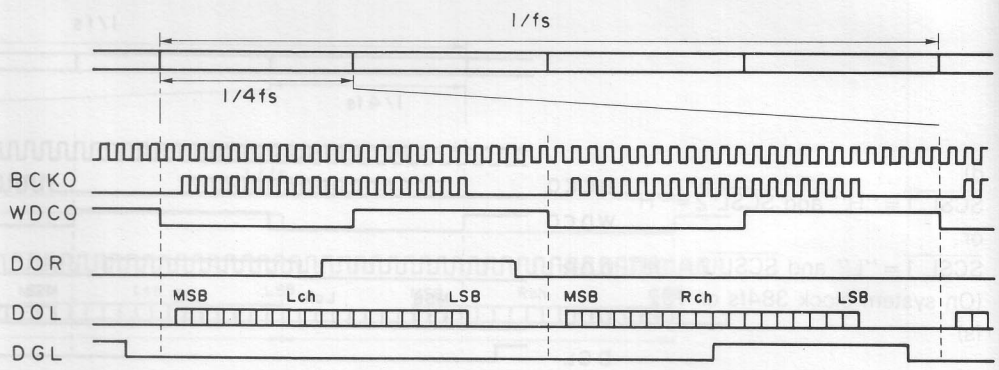


i)
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 256 fs)

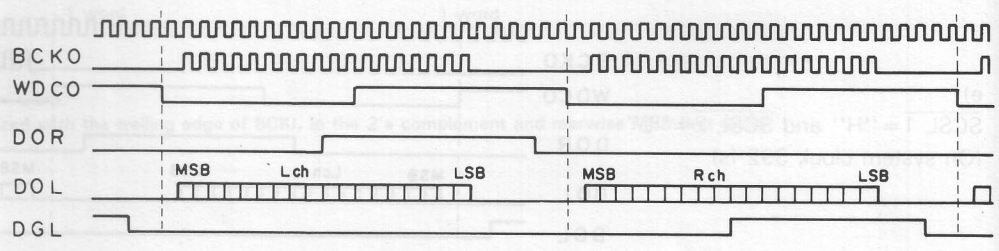


(4) 18-bit mode: $\overline{\text{SOMD 1}}$ = "L" and $\overline{\text{SOMD 2}}$ = "L"

j)
$\overline{\text{SCSL 1}}$ = "H" and $\overline{\text{SCAL 2}}$ = "H"
or
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 384 fs or 192 fs)



k)
$\overline{\text{SCSL 1}}$ = "H" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 392fs)



l)
$\overline{\text{SCSL 1}}$ = "L" and $\overline{\text{SCSL 2}}$ = "L"
(On system clock 256fs)