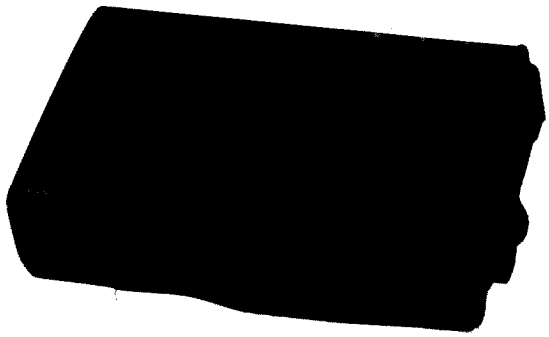
NEW TECHNICAL THEORY
FOR SERVICING

TCD-D8
CIRCUIT OPERATION
(BASIC OPERATION, CIRCUIT OPERATION)



DIGITAL AUDIO TAPE RECORDER

SONY®

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BASIC OPERRATION

CIRCUIT OPERATION

CHAPTER 1. DIGITAL AUDIO TAPE RECORDER SYSTEM

The digital audio tape recorder system is normally called DAT system, by taking its initials.
This chapter describes this DAT system, its mechanism, and merits.

1.1 What is DAT

DAT is a system which recounts sound waveform using binary numbers "1" and "0" (by **digitalization**) to record on and play back tapes. This chapter will mainly describe the rotary head digital audio tape recorder DAT (**R-DAT**: Rotary Head Digital Audio Taperecorder) which was commercialized in March 1987 and is currently the most widely used DAT system. The features of this DAT system are as follows.

(1) 16-bit multi fs
- 16-bit linear quantization → high sound quality equivalent to CDs, and applicable for non-consumer uses as well
- 48k, 44.1k, 32 kHz sampling frequencies (fs)
  → Directly digital-connectable to various types of digital equipment

(2) High density recording
- Helical scan method using rotary head
  → ø 30 (15) mm drum, Ach/Bch (2 heads)
- Guard bandless azimuth recording → Recording density 114 MBPI²
- 90° lap mechanism discontinuous recording by time axis compression

(3) High reliability
- Highly efficient error correction coding (Duplex Reed-Solomon code)
- Block-complete interleave → Completed with 2 tracks, numerous functions for editing
- ATF tracking servo → Fixed head (CTL head) not required
- Overwritable → Erasure head not required

(4) Multiple functions
- High sub-code area → Start ID, program No., etc. (200 Kbits/s)
- Area-divided format → After-recordable sub-code
- High speed access by 90° lap shallow-winding mechanism
  (x200 faster than playback in some models)

(5) Compact cassette
- Use of metal tape and flangeless cassette enables continuous recording for two hours
- Completely sealed structure incorporating hub brake system and end detection prism

(6) Wide application
- Applicable to Walkman, HiFi audio, Non-consumer data recorder
- Various uses with extended play, 4 channels, wide track, etc.
  → Takes into consideration diverse needs and mass production of software tapes.

1.2 Analog Recording and Digital Recording

1.2.1 Analog Recording

The conventional tape recorder, as shown in **Fig. 1.1**, converts amplitude waveform of sound signal currents directly to magnetic flux density*1 proportionate to the amplitude of the current. The magnetic flux density of the tape is also taken as the changes in the current in playback. Consequently, when large amplitude currents are supplied, magnetic saturation*2 prevents proportionate magnetic flux density from being obtained, causing sound distortion and small amplitudes to be hidden behind tape noises. Moreover, the driving force of the tape has slight rotation inconsistency, thus leading to irregular speed of tape running and to wow flutter*3 in which the sound is vague or shaky.
There is, therefore, a limitation to performance with analog playback which records and plays back sound signal currents continuously and regardless of the amplitude.

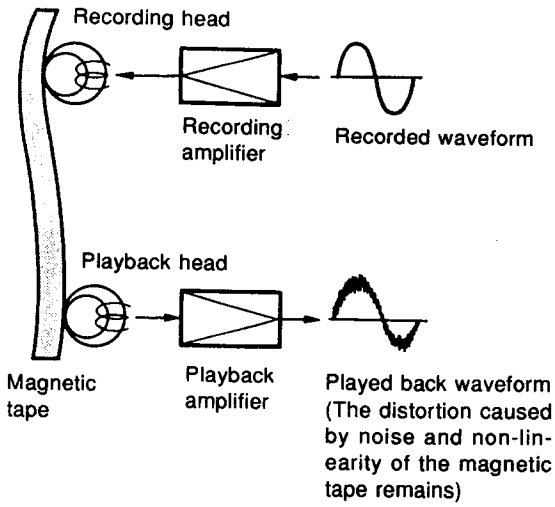


Fig. 1.1 Analog Tape Recording/Playback System

*1...Magnetic density : The magnetic lines of force from the magnet are drawn from the N pole to the S pole, and are believed to flow together in a mass. This is called magnetic flux. The amount of magnetic flux per unit area (1 m^2) is called magnetic flux density.

*2...Magnetic saturation : The magnetic flux density increases proportionately to the strength of the magnetic field until a certain level, beyond which it will not increase even if the magnetic field is made stronger. This phenomenon is called magnetic saturation.

*3...Wow flutter : Wow flutter is the changes in the speed of the tape in the tape recorder or the rotating speed of the record player in a certain period.

1.2.2 Digital Recording

With the digital recording format, continuous sound waveform signals are divided according to as shown in the top drawing of **Fig. 1.2**, and the amplitude of the waves is remeasured by binary numbers "1" and "0", where "1" is taken as "current flows" while "0" is taken as "no current flows", and the signals are recorded on the magnetic tape as "magnetic changes " and "no magnetic changes". During playback, this presence/absence of magnetic changes on the tape corresponds to the presence/absence of current flowing to the coil, and the amplitude of the current is calculated to reproduce the original sound signal currents.

During this process, between recording performed with the recording head and playback with the playback head, only **"presence/absence of current"** and **"presence/absence of magnetic changes"** will be taken into consideration in recording and playback. Therefore even if distortion and noises mix and disturb the waveform, or the rotation becomes inconsistent and disturbs the waveform, as long as the waveform is rectified to the original waveform as shown at the bottom of **Fig. 1.2**, the sound signal waveform can be reproduced correctly. This is one of the greatest feature of digital recording.

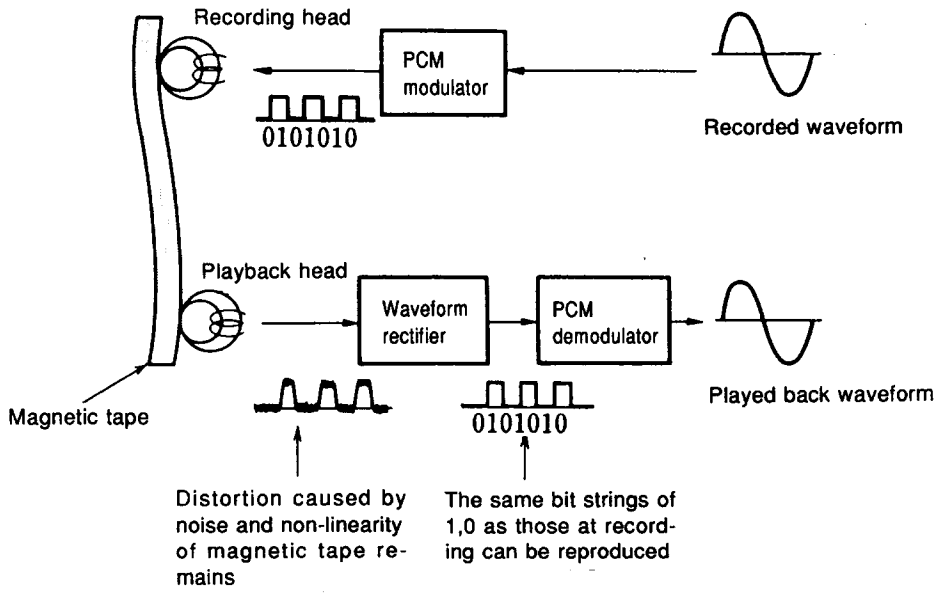


Fig. 1.2 Digital System Tape Recording/Playback System

1.3 Digitalization Procedure

1.3.1 Digitalization of Waveform

First sound signal waveform is converted to binary numerical rows. As shown in **Fig. 1.3**, how closely the original waveform can be reproduced depends on how much interval to leave between the sound signal waveform (**sampling**) and how accurately the waveform is read (**quantization**).

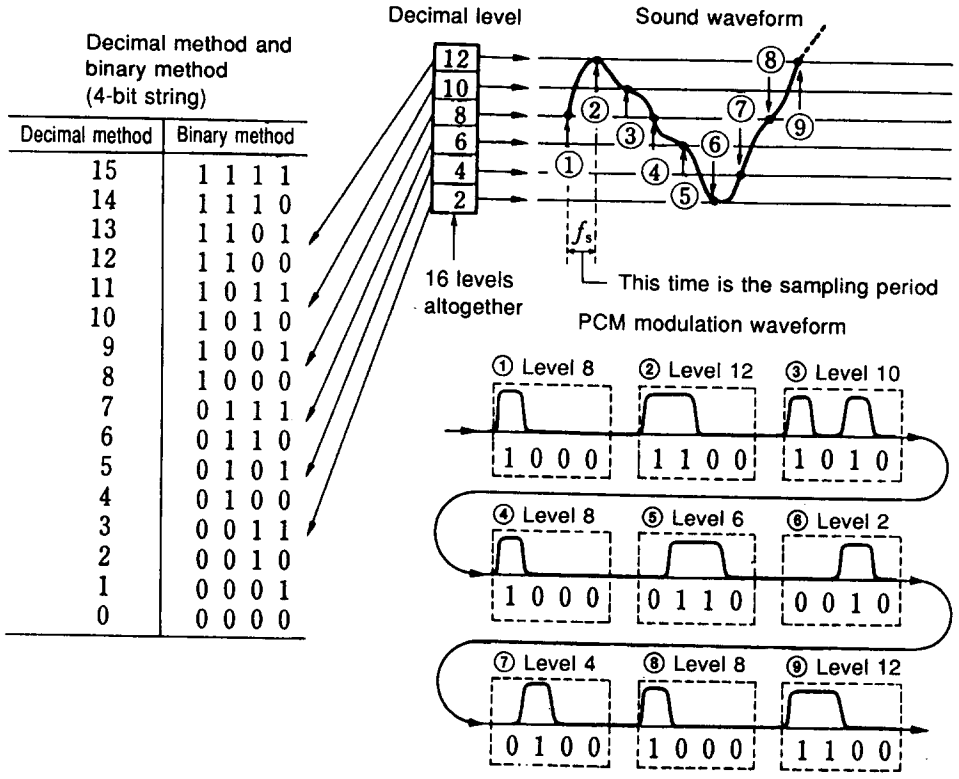


Fig. 1.3 Sound Signal Waveform (Analog) Digitalization Processing Procedure

1.3.2 Sampling

Sampling means how minutely the horizontal time axis of the sound signal waveform is divided. The number of waveform read in one second is called the sampling frequency (fs is the symbol). To reproduce the waveform as closely as possible, it is necessary to divide and read the changes as minutely as possible so that these changes can be tracked. As a rough approximate, **it has been recommended that a sampling frequency more than twice the frequency of the sound waves to be reproduced be selected**, according to the sampling theorem.

For example, if the sampling frequency is set as 48 kHz (the sound waveform in one second is divided into 48000 and read), 1/2 of this (24 kHz) becomes the upper limit of the playback frequency range. Consequently, the sound signals below this frequency can be more or less reproduced closely, but not for signals above this frequency.

1.3.3 Quantization

Quantization means how minutely the amplitude of vertical axis of sound waveform signals is divided in binary.
When between the maximum positive and negative values of sound waves are quantized for example, **Fig. 1.4** shows when quantization is performed with 2 bits (represented by a combination of two "0"s and "1"s), **Fig. 1.5** shows when quantization is performed with 3 bits (represented by a combination of three "0"s and "1"s.)

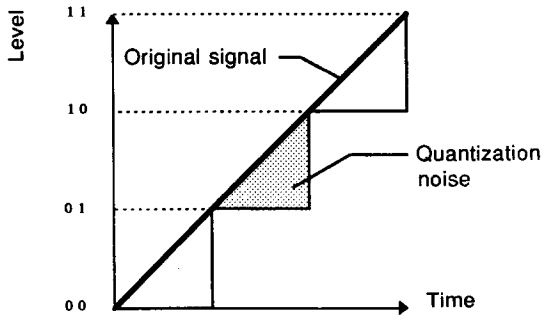


Fig. 1.4 2-Bit Quantization

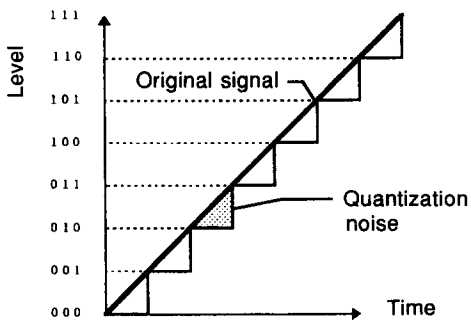


Fig. 1.5 3-Bit Quantization

As shown in the above figure, the value after quantization is not the actual amplitude of the original signal waveform for the difference in the amplitude of the original signal. This difference is called the quantization noise (or quantization distortion). It is a type of noise peculiar to the digital system which always occurs during digitalization.
The size of this quantization noise decreases as the quantization bit is increased. The scale accuracy doubles as the bit increases by one so that the difference with the amplitude of the original signal becomes 1/2.
For example, if 16-bit linear quantization is performed, the scale becomes as detailed as $2^{16} = 65536$.
For this reason, the method of quantization which measures the amplitude of the original signal at equal intervals using a binary scale is called **linear quantization. Fig. 1.6** shows the input/output characteristics of linear quantization.

In respect to this, to divide the strength of a certain sound with a few bits (to use as little bits as possible), taking into consideration the nature of the hearing of human beings and the nature of sound signals, as shown in **Fig. 1.7**, the scale is made fine where the amplitude is small and rough where the amplitude is great. This is called **non-linear quantization.** With non-linear quantization, the quantization noise is small at small signal levels and great at high signal levels, and the noise level changes according to the input signal level. These methods are adopted because noises which increase to a certain level when signal levels are high cannot be heard by the hearing of human beings.

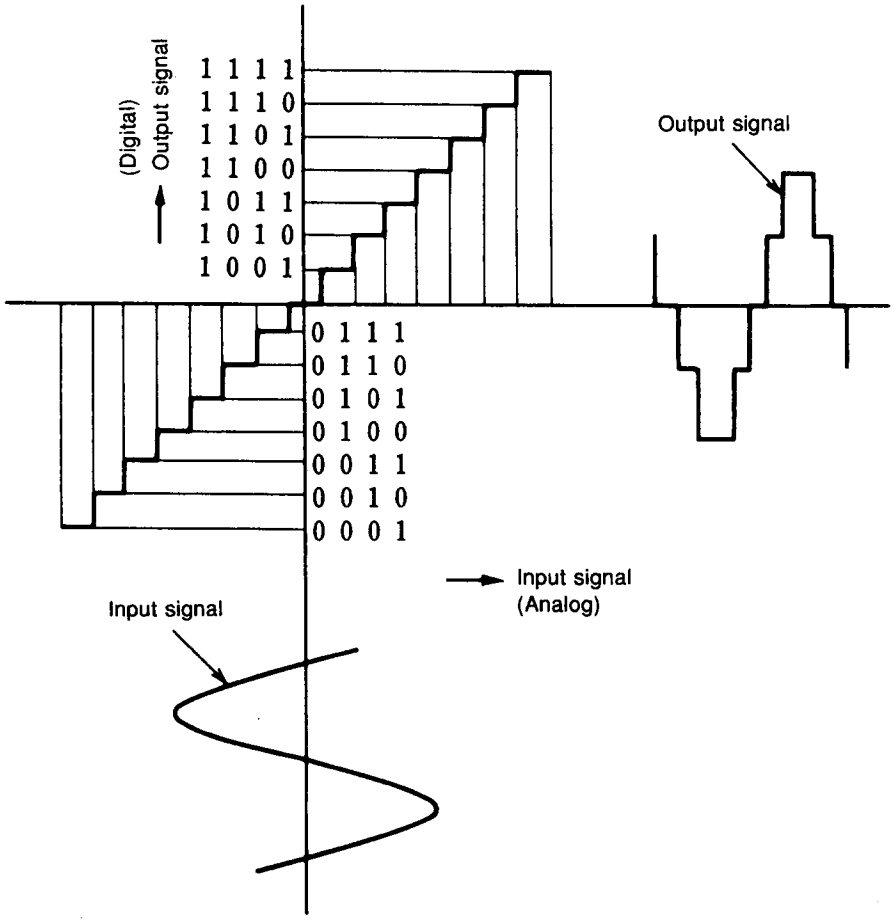


Fig. 1.6 Input/Output Characteristics of Linear Quantization

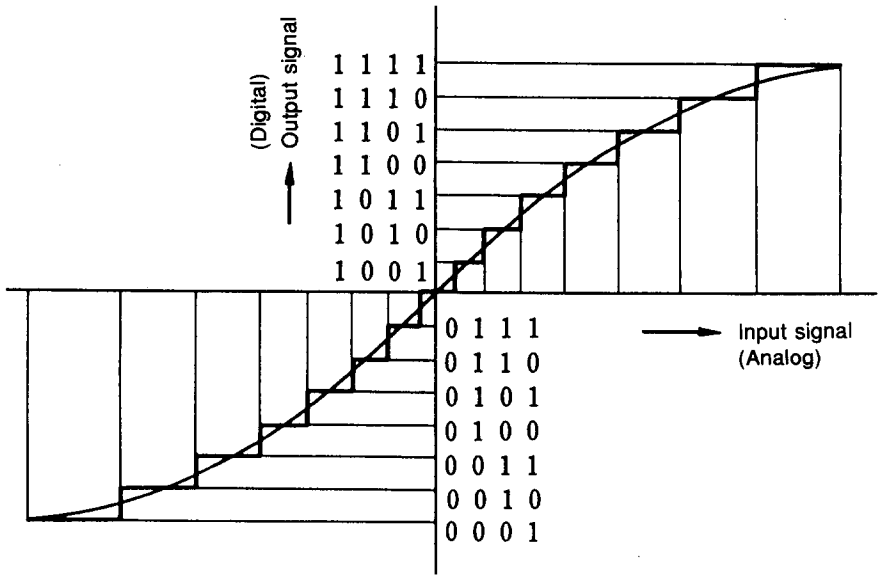


Fig. 1.7 Input/Output Characteristics of Non-Linear Quantization

CHAPTER 2. DAT (R-DAT) SYSTEM STANDARDS

This chapter describes the main standards of DAT.

2.1 Main Standards of DAT

2.1.1 DAT Mode

The DAT system has six modes as shown in **Table 2.1**. The features of these six modes are described in the following. **Take note that, unlike analog recording, no sounds will be played back in digital recording if the wrong mode is used.**

(1) 48k mode:The recording and playback standard mode and sampling frequency is 48 kHz, the quantization bit number is 16 bits, and linear quantization is used.
The tape speed is 8.15 mm/s, enabling two hours of continuous recording. Most of the DAT systems are equipped with not only analog input/output but digital input/output as well, enabling mutual digital dubbing.
◎Best suited for satellite broadcast B mode recording and playback.

(2) 44k mode:Recording and playback enable. The sampling frequency and quantization bit are the same as CDs. The tape speed and recording time are the same as the 48k mode.
◎Best suited for recording and playback of CD and MD software discs and DAT software tapes.

(3) 44k-WT mode: **Playback only mode**. WT stands for Wide Track Pitch. In this mode, the tape speed is 1.5 times the standard speed which is 12.225 mm/s. The track width is also expanded by 1.5 times. This mode is provided especially for contact printing, which can be applied for the mass production of software tapes. The insufficient output of the contact-printed tapes is supplemented by widening the track width. The playback time is 80 minutes.

(4) 32k mode:Optional mode. The sampling frequency is 32 kHz and the quantization bit number is 16 bits. Linear quantization is used. It enables recording to be performed
without degrading the quality of the PCM broadcast in any way.
As the tape speed is 8.15 mm/s, recording and playback of two hours can be performed.
Suitable for recording signals input from digital inputs directly.
◎Best suited for the recording and playback of the satellite broadcast A mode.

(5) 32k-LP mode:Optional mode. LP stands for Long Play.
The sampling frequency is 32 kHz and the quantization bit number is 12 bits. Non-linear quantization is used.
By compressing the quantization bit number to 12 bits, the recordable time is doubled to four hours.
Compared to the standard 48 kHz and 16 bits, the 32 kHz and 12 bits information volume per channel is exactly half from the following, thus enabling extended recording of two times.
48 kHzx16 bits = 78 kbits/s = 2x32 kHz x12 bits

(6) 32k-4ch mode:Optional mode. Pair mode with 32k-LP mode.
The information volume decreased by adopting 12-bit non-linear quantization is used for increasing the number of channels.
This mode has the same tape speed as the 48k mode, enabling the recording of signals of 4 channels.

2.1.2 Comparison with Compact Cassette Tape

Compared to the tape speed of analog compact cassette tape speed (4.76 cm/s);
① Relative speed: About 66 times with 3.13 m/s → High density recording (See **Fig. 2.1**)
② Tape speed: About 1/6 times with 8.15 mm/s → Low tape consumption amount, high speed FF/REW (See **Fig. 2.2**)

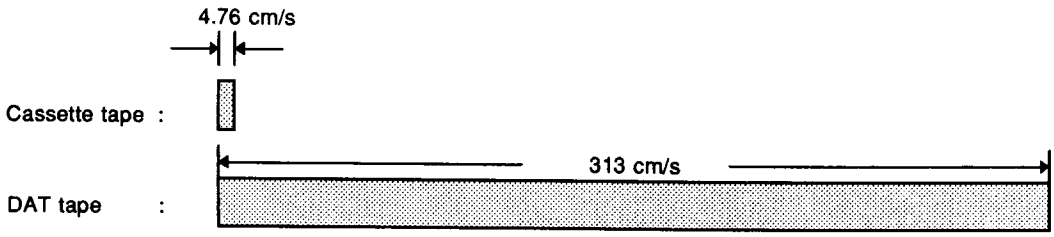


Fig. 2.1 Comparison of Cassette Tape and DAT Tape Relative Speeds

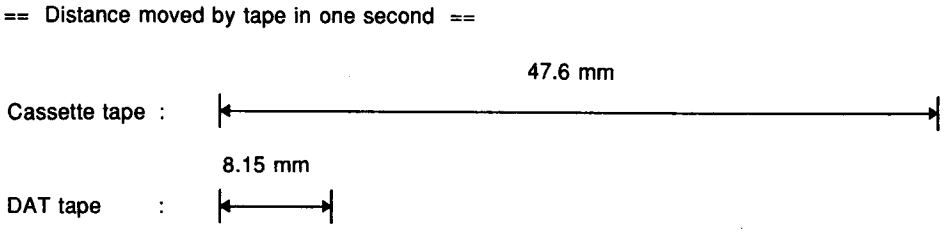


Fig. 2.2 Comparison of Cassette Tape and DAT Tape Speeds

Table 2.1 Main Standards of Modes Used in DAT Systems

Item \ Mode	Recording and Playback Mode					Playback Only Mode
	48k mode	32k mode	32k-LP mode	32k-4ch mode	44k mode	44k-WT mode
Channel no. (ch)	2	2	2	4	2	2
Sampling frequency (kHz)	48	32	32	32	44.1	
Quantization bit no. (bit)	16 (Linear)	16 (Linear)	12 (Non-linear)	12 (Non-linear)	16 (Linear)	16 (Linear)
Linear recording density (kbpi)	61.0	61.0			61.0	61.1
Plane recording density (kbpi^2)	114	114			114	76
Transmission rate (Mbps)	2.46	2.46	1.23	2.46	2.46	
Sub-code capacity (kpbs)	273.1	273.1	136.5	273.1	273.1	
Modulation method	8-10 modulation format					
Correction method	Duplex Reed-Solomon code					
Tracking method	Area divided ATF					
Cassette size (mm)	73x54x10.5					
Recording time (min)	120	120	240	120	120	80
Tape width (mm)	3.81					
Tape type	Metal powder					Oxidation tape
Tape thickness (μm)	13±1					
Tape speed (mm/s)	8.15	8.15	4.075	8.15	8.15	12.225
Track pitch (μm)	13.591				13.591	20.41
Track angle	6° 22′ 59.5″					6° 23′ 29.4″
Standard drum specifications	ø 30 90° lap					
Number of rotation (r.p.m.)	2000		1000	2000	2000	
Relative speed (m/s)	3.133		1.567	3.133	3.133	3.129
Head azimuth angle	±20°					
Remarks	Standard recording and playback mode	PCM broadcast recording	Extended recording Half-speed	4ch	44.1 standard mode	Music tape only mode, suitable for contact print, playback only
Current general DAT — Recording — Analog	O	X	O	X	X*1	X
Current general DAT — Recording — Digital	O	O	O	X	O	X
Current general DAT — Playback	O	O	O	X	O	O
Characteristics — Frequency response	22 kHz	14.5 kHz	14.5 kHz	14.5 kHz	20 kHz	20 kHz

*1: DTC-A7, DTC-A8, DTC-60ES, DTC-2000ES, and TCD-D8 can record at sampling frequencies of 44.1 kHz.

2.2 Rotary Head Method (R-DAT)

2.2.1 Azimuth Guard Bandless Recording Method

The azimuth guard bandless recording method is the best method for increasing recording density.
To explain the theory briefly;With the current recording method using the guard bands, as shown in **Fig. 2.3**, to prevent the mixing of signals by tracking deviation during playback due to the recording of heads A and B at the same angle, guard bands are used to create space.

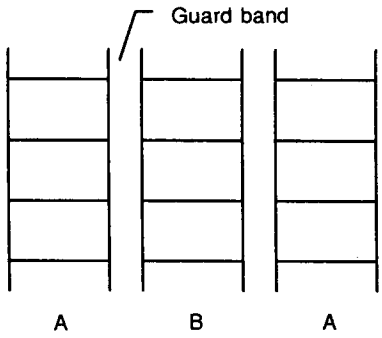


Fig. 2.3 Recording Method Using Guard Bands

With the azimuth guard bandless recording method, by tilting heads A and B in the opposite direction to the direction in which they move as shown in **Fig. 2.4**, signals of track B will not be played back by head A and the signals of track A will not be played back by head B, thus preventing the mixing of signals. This makes the guard band between tracks A and B redundant, increases the track pitch, and consequently increases the recording density.

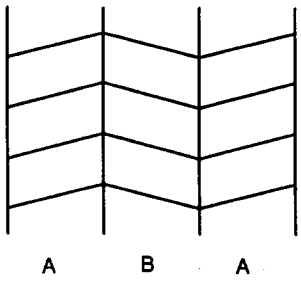


Fig. 2.4 Azimuth Guard Bandless Recording Method

The features of the azimuth guard bandless recording method are shown below.
① Resistant to tracking error and mechanism accuracy is not critical
② Suited for overwriting
③ Suited for ATF method

The azimuth guard bandless recording method is capable of increasing the track width for recording and playback heads above the recording track pitch as shown in the left figure of **Fig. 2.5** (because of guard bandless).
It is advantages in terms of compatibility because during playback, as the playback head width is wider than the track pitch, even if the tracking deviates slightly, sufficient output can be obtained. (See **Fig. 2.5**. Right Figure)

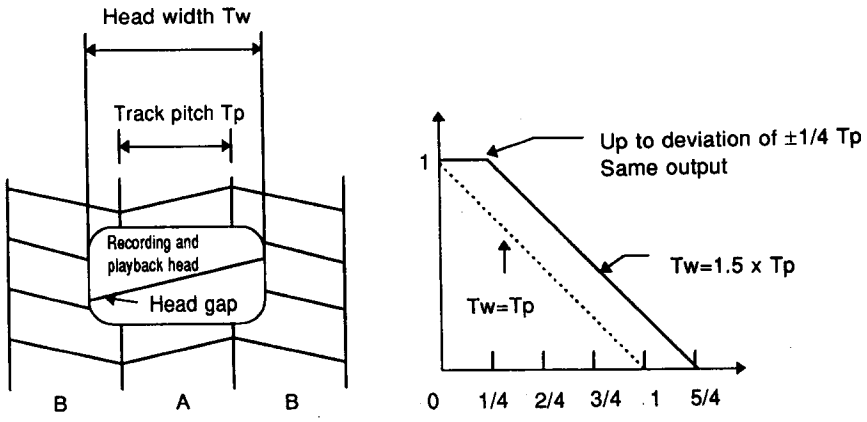


Fig. 2.5 Output Characteristics of Guard Bandless Recording and Wide Head

The ATF method which performs tracking by reading signals from adjoining tracks simultaneously can be performed without the need of special heads. Because the head width is wider than the recording track width, complete erasure is ensured as shown in **Fig. 2.6**, thus ensuring overwriting without any erasure heads.

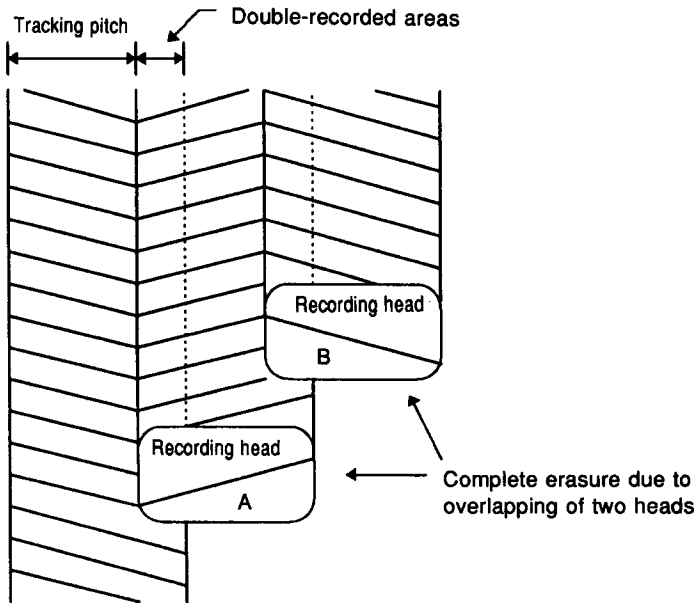


Fig. 2.6 Recording

2.2.2 Helical Scan Method

To realize further decrease in size and easy-to-use drum speed for the rotary head of the DAT system, the **helical scan method (tilted scanning)** which has been used most extensively in previous VTR models has been adopted.

With the helical scan method, the track is slightly tilted against the tape running direction to form a long linear track. The merits of this method are;

① As the drum is slightly tilted against the tape, safe tape running and contact between tape and head can be expected.
② Large diameter drums can be used with a comparatively low speed, etc.

As the track of this method is linear, systems can be designed with any drum diameter. The drum diameter is described in more detail in the following.

2.2.3 Drum Diameter

Currently, the drum diameter of the DAT system is ø 30 mm with a lap angle of 90° for installed units and ø 15 mm with a lap angle of 180° for portable units. This is because the variation of the drum diameter is prescribed as follows.

øχ [mm], 2700°/χ lap angle

(Note) ø : Indicates the diameter.

Take for example the installed unit, as the diameter is 30 mm, when x is substituted with 30, the lap angle becomes 2700/30 = 90°, thus the system has a drum diameter of ø 30 mm with a lap angle of 90°.
In this way, the system can be designed with an drum diameter as shown above.

2.2.4 Definition of Track Pattern

With the DAT format, the track pattern recorded on the tape is defined as shown in **Fig. 2.7**. As heads A and B perform recording once each with every one rotation of the drum, the track pattern is such that tracks A and tracks B are lined up orderly.

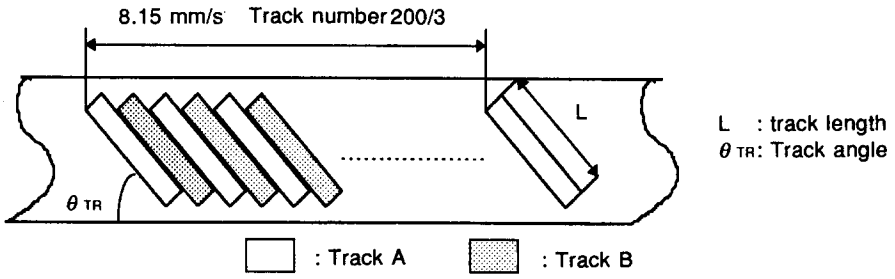


Fig. 2.7 DAT Track Pattern

With the current DAT which uses a head drum with a diameter of 30 mm, this track pattern is realized with the following specifications;
Number of head drum rotations:2000 rpm
Angle of tape winding around the head drum:90°
Angle of tilt of tape winding around the head drum in helical form (still angle θ) : 6° 22′.
The signal waveform is an intermittent signal (**discontinuous signal**) which always appears at the blank portion between the signals of track A and track B (See **Fig. 2.8**.) because the tape winds around the head drum only for 90°.
Even if data is read from the tape discontinuously, by accumulating it in proper order on the memory and sending this data sequentially to the D/A converter, the signal can be played back as a continuous music signal. This is one feature of the DAT which records in digital.

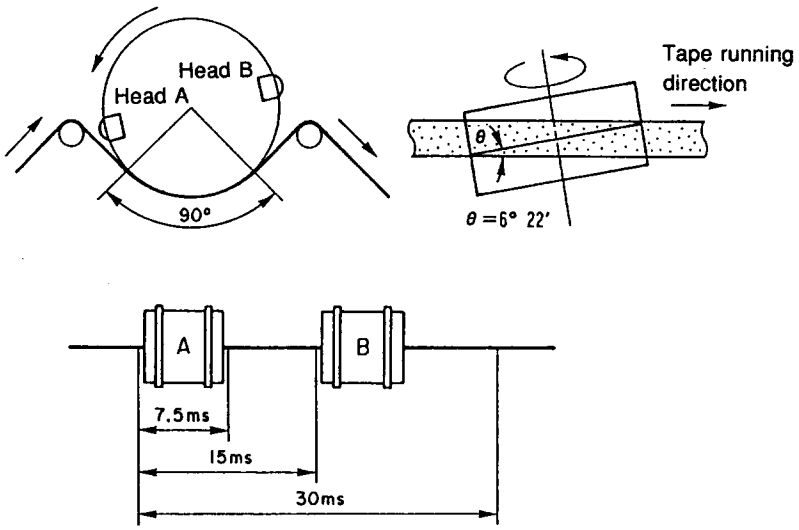


Fig. 2.8 Drum with Diameter 30 mm

When using a head drum with a diameter of 15 mm, first to equalize the track length, since the diameter of the drum is 1/2, it is necessary to set the winding angle to 180° which is two times that of the head drum with a diameter of 30 mm. (ø 15 mm, lap angle of 180°) Next, the drum is rotated at a speed of 2000 rpm , as with the drum with a diameter of 30 mm. In this case, as the relative speed is 1/2, the track angle ø in **Fig. 2.10** is greater than that of the drum with a diameter of 30 mm. Therefore, the required track angle cannot be obtained with the same still angle θ as the drum with a diameter of 30 mm.

Consequently, with the head drum with a diameter of 15 mm, the still angle θ is made smaller than the drum with a diameter of 30 mm by about 1′.

On the other hand, the signal waveform has a shape made by expanding the waveform of the drum with a diameter of 30 mm in the time axis direction by two times as shown in **Fig. 2.9** and filling the blank portion. The basic frequency of the signal is 1/2. However, in this case, although there is a need to change the timing for reading the data from the tape, by arranging the data read on the memory, after that only the data need to be sent to the D/A converter sequentially, which makes it no different as when the drum with a diameter of 30 mm is used.

(Note) rpm : Indicates the rotation per minute.

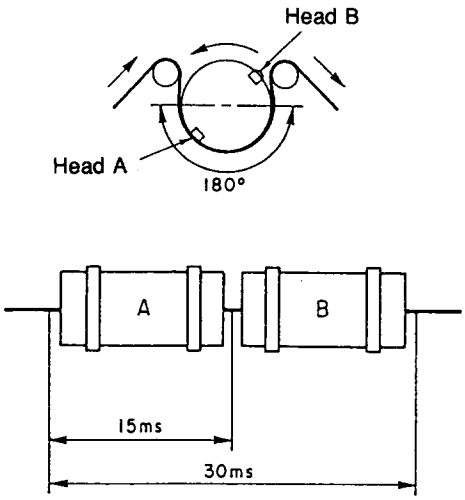


Fig. 2.9 Drum with a Diameter of 15 mm

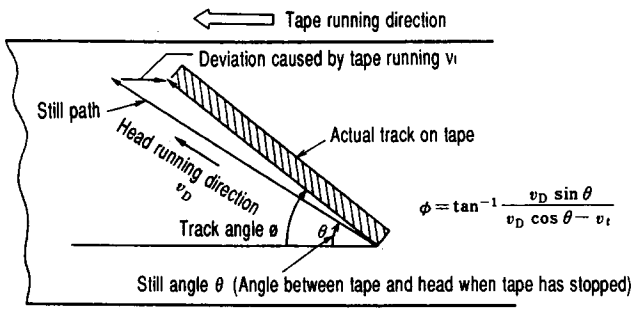


Fig. 2.10 Relation Between Track Angle and Still Angle

2.3 DAT Tape Format

Fig. 2.11 and **Table 2.2** show the DAT tape format.
First, the basic tape width (A in the figure) is $3.81^{+0}_{-0.02}$ mm, the same tape width as the compact cassette recorder which many of us are familiar with. With the DAT system that requires precise tape running, the width tolerance standard is extremely strict, more than two times that of the compact cassette.
The effective recording width (W in the figure) is the width with which the rotary head actually records signals (approximately 2.61 mm). This means that the 0.5 mm at both edges is not used and remains as optional tracks.
With the rotary head method, the two edges of a tape is normally not used. This is because the conditions for contact between the tape and head change at the edge of the tape, resulting in difficulty in achieving safe contact between the tape and head. In addition, tape edges damage easily and data errors occur frequently.
The DAT format has high capacity by taking into consideration all of these points.
The track angle which is the most important is 6° 22′ 59.5″, and is used for all modes except the 44k-WT mode. In the 44k-WT mode, because the tape speed is 1.5 times faster, the track angle differs slightly. These measurements are all based on the lower edge of the tape. Normally, drums are equipped with a precision guide (called lead) to preserve this angle, and the tape pattern is created by having the lower edge of the tape ride onto this lead.

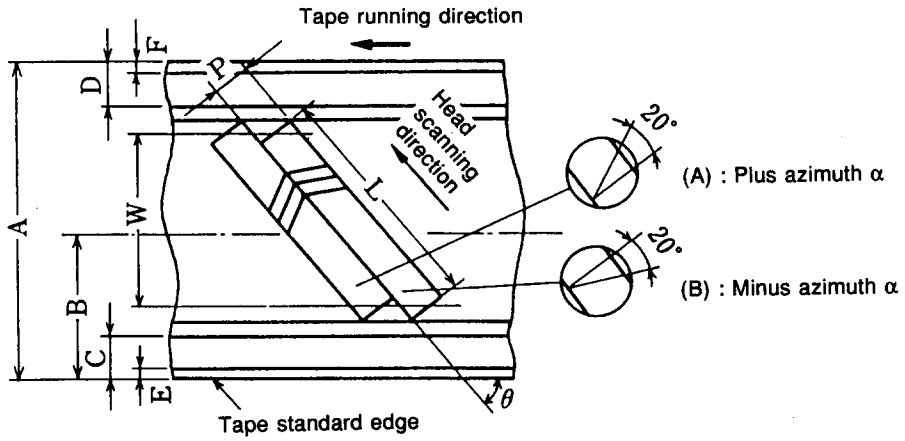


Fig. 2.11 DAT Tape Format

Table 2.2 DAT Tape Format

		48k mode, 44k mode, 32k mode, 32k-LP mode, 32k-4ch mode	44k-WT mode
A	Tape width (mm)	3.81 (+0, –0.02)	
W	Effective recording length (mm)	2.613	
L	Track length (mm)	23.501	23.471
P	Track pitch (μm)	13.591	20.41
B	Track center (mm)	1.905	
C	Optional track I (mm)	0.5	
D	Optional track II (mm)	0.5	
E	Edge guard I (mm)	0.1	
F	Edge guard II (mm)	0.1	
θ	Track angle (deg.)	6° 22′ 59.5″	6° 23′ 29.4″
α	Head gap azimuth angle (deg.)	±20° (±15′)	

2.4 Arrangement of Signals on Track

With the DAT system, various signals are written on one track by dividing it into different areas. As shown in **Fig. 2.12**, one track is divided mainly into seven areas, and each of these areas are further divided as shown in **Table 2.3**. One merit of the DAT format is that editing can be performed freely by having the following independent areas.

- Main area for recording audio data
- Sub area for recording the program-search signal
- ATF area for recording the ATF signal for tracking

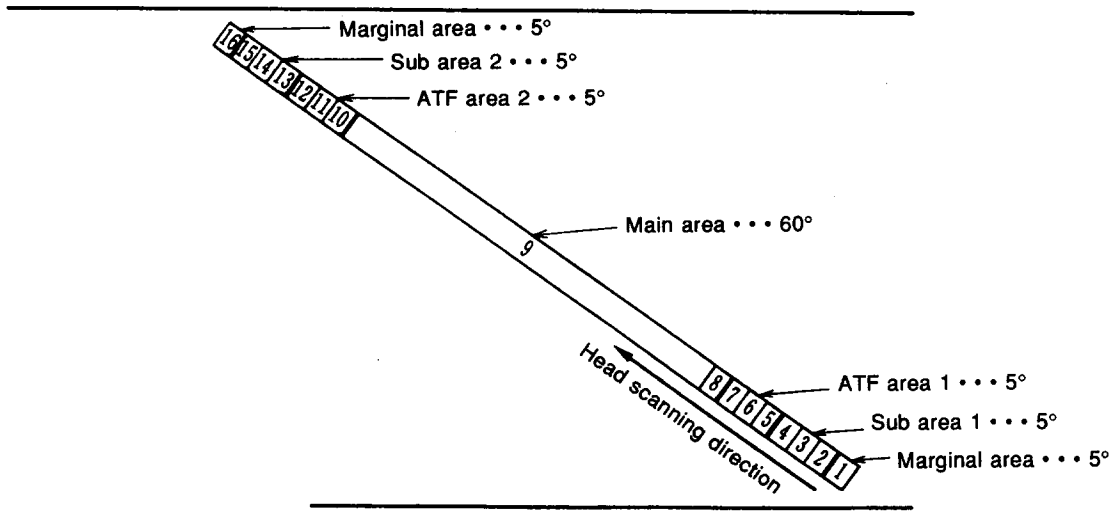


Fig. 2.12 Data Arrangement on DAT track

Table 2.3 Signal Arrangement on Track

Fig. No.	Area Name	Contents	Signal	Angle*1 (deg.)	Block No.	Time (μS)
1	Marginal area	Margin 1	1/2 fch*3	5.051	11	420.9
2	Sub area 1	Preamble 1	1/2 fch	0.918	2	76.5
3		Sub data area 1		3.673	8	306.1
4		Postamble 1	1/2 fch	0.459	1	38.3
5	ATF area 1	IBG*2 1	1/6 fch	1.378	3	114.8
6		ATF 1		2.296	5	191.3
7		IBG 2	1/6 fch	1.378	3	114.8
8	Main area	Preamble 2	1/2 fch	0.918	2	76.5
9		Main data area		58.776	128	4898.0
10	ATF area 2	IBG 3	1/6 fch	1.378	3	114.8
11		ATF 2		2.296	5	191.3
12		IBG 4	1/6 fch	1.378	3	114.8
13	Sub area 2	Preamble 3	1/2 fch	0.918	2	76.5
14		Sub data area 2		3.673	8	306.1
15		Postamble 2	1/2 fch	0.459	1	38.3
16	Marginal area	Margin 2	1/2 fch	5.051	11	420.9
	Total			90	196	7500

*1: These figures are for the ø 30, 90° lap drum rotated at 2000 rpm

*2: IBG: Inter Block Gap. Margin space between blocks containing information recorded on the tape

*3: Channel clock (fch=9.408 MHz) serving as standard for data recording

The role of each of these areas of a track is described below.

(1) Marginal area

This area is located about 5° at both edges. It is a spare area provided to attain stable contact between the tape and head. No signals are recorded.

(2) Sub areas 1 and 2

A unique function of the DAT system, these areas are used for recording the sub-code signals (various signals such as time and address). The preamble is attached before the data signal and the postamble after the data signal. These signals are used for synchronizing with the PLL (phase locked loop) and erasing previous data in after-recording. These areas cover 5° of space in total, of which 3.7° is used for recording signals.

The sub area is divided into two areas to;

- Deal with burst error
- To make reading of data easy during high speed search

(3) ATF areas 1 and 2

These areas are recorded with the ATF (automatic track following) signals for tracking detection, which will be explained later.

Before and after the ATF signals, IBG (inter block gap) is provided . The IBG serves to;

- Prevent the erasure of the ATF signals even when there is signal deviation
- Cover the switching time of the recording and playback modes of the head.

(4) Main area

Made up of about 60°, this area is used for recording audio data converted to main digital data. It is also recorded with the parity for the audio data error correction, and the main ID (part of sub code) which records the audio data format.

CHAPTER 3. DAT ERROR CORRECTION

This chapter describes the basic concept of error correction, the most important point in handling digital data, and the error correction method used in the DAT system.

3.1 ERROR CORRECTION METHOD AND INTERLEAVE

3.1.1 Why Error Correction is Important

The following shows why error correction is important in the handling of digital data. As shown in **Fig. 3.1**, for "1000" which represents "8" digital data (binary data) in the decimal order, if the higher most bit "1" is mistaken as "0", the "1000" data will be mistaken as decimal "0" data in the form of "0000". In this way, as all the data will become incorrect just by mistaking one bit, error correction is has great importance.

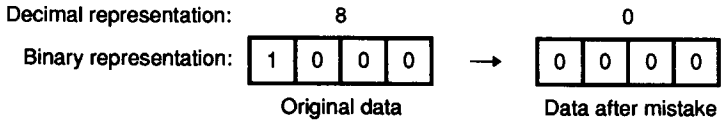


Fig. 3.1 Example of Error

3.1.2 Characteristic of Error Correction Code

The ability to completely correct data errors caused by scratched and failed tapes and discs is already familiar with CDs. In the case of DAT, the error rate per bit is 10^{-5} to 10^{-6} on the average. If 1.5M bits of audio data is recorded every second, it means that errors occur several times each second.

The characteristic of the error correction code is explained here briefly. As shown in **Fig. 3.2**, data for correction (k bit) is added to the data signal (n-k bit), and the correct data pattern is sent together with the n bit data containing the error pattern. But if errors occur halfway through the transmission, the data being sent will appear as various failed data, and this difference in how it appears is called distance.

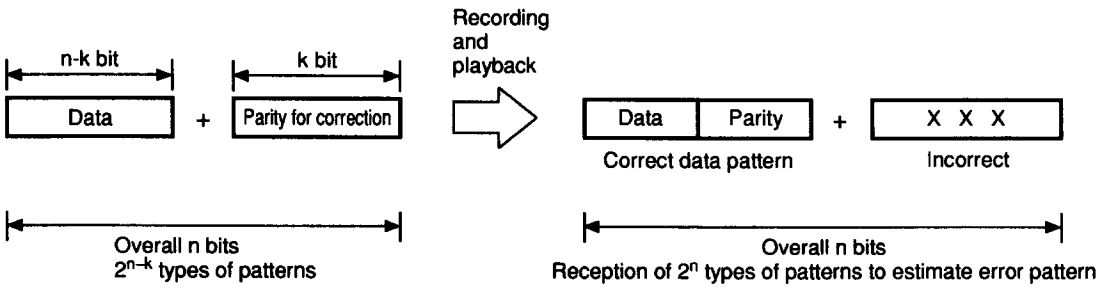


Fig. 3.2 Error Correction Coding Process

For example, if the transmission side data and reception side data differ at four locations as shown in **Fig. 3.3**, the distance will be "4". This distance is calculated at the reception side, the error position is determined, and error correction is performed.

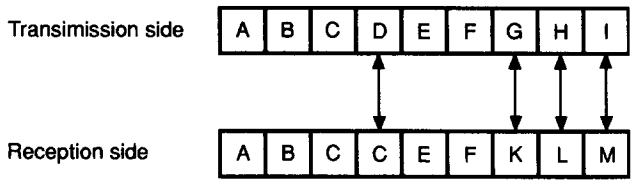


Fig. 3.3 Distance Between Data

3.1.3 Interleave

There are broadly two types of error patterns-random error and burst error. These are described briefly in the following.

- Random error ..... As shown in **Fig. 3.4** (a), these errors are generated independently, mainly due to the noise components.

- Burst error ..... As shown in **Fig. 3.4** (b), these errors are generated continuously, mainly due to the failure and scratching of tapes, and deviation of synchronization.

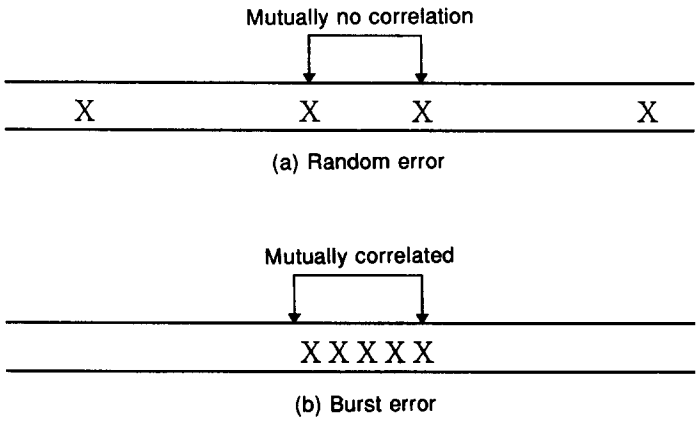


Fig. 3.4 Random Error and Burst Error

If errors occur continuously as with burst errors, a certain portion of the data will be lost to a considerable extent, consequently leading to difficulty in correction and compensation. The method thus used in such cases is interleave. The basic concept of interleave is described next.

Interleave means the work to rearrange signals according to a certain rule (method to record a group of data not together but one by one).

As shown in **Fig. 3.5**, as (a) and (b) are rearranged, if the burst error occurs, and it is corrected to the actual signal (de-interleave), several small random errors will be generated in scattered form as shown in (c), and thus enable the error to be estimated from the redundancy bit, and the correction shown in (d) to be performed.

If error cannot be corrected, the actual value can be estimated from the previous and following data, since the original data is an analog signal.

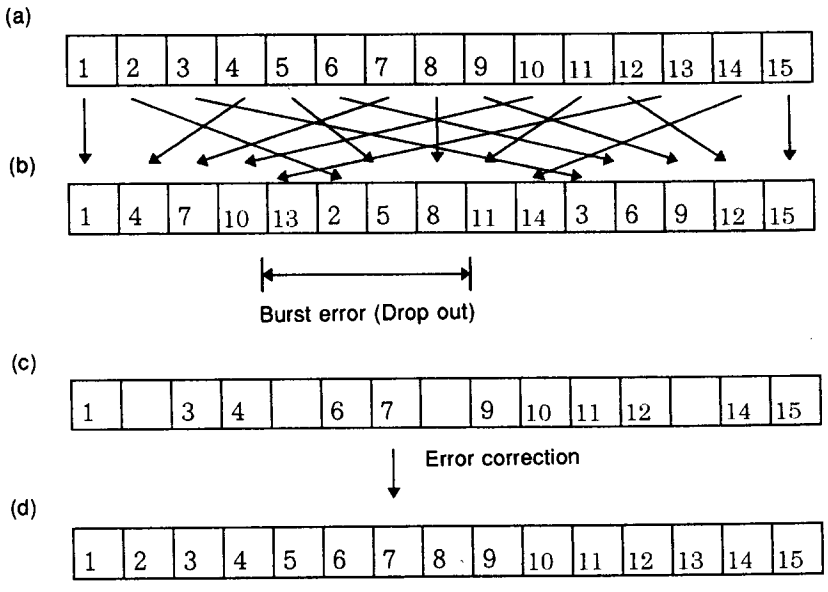
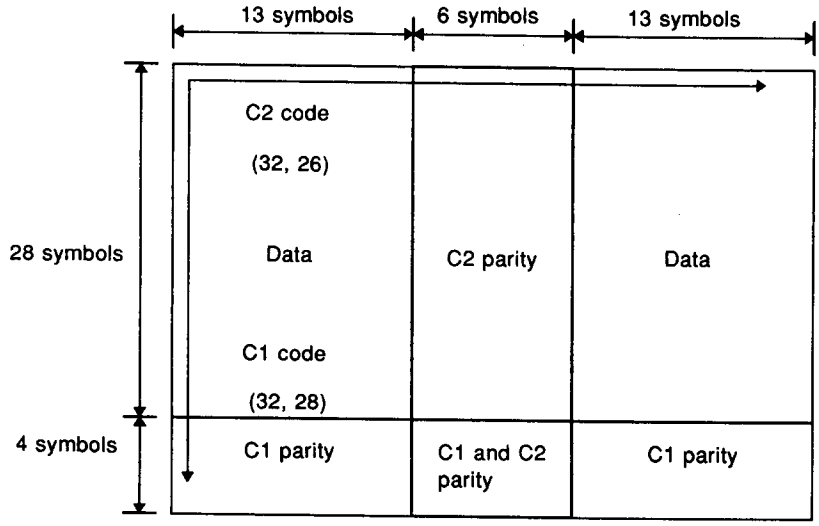


Fig. 3.5 Concept of Interleave

3.2 Duplex Reed Solomon Code

This chapter describes the **duplex Reed Solomon** method used by the DAT system.
As shown in **Fig. 3.6**, two Reed Solomon codes are combined in the vertical and horizontal directions in the DAT system. This combination is called product code.



Duplex Reed Solomon Code

(Note)1 symbol = 8 bits

Fig. 3.6 DAT Product Code Structure

Combining two codes in this way creates stronger resistance to random error, and enables the creation of practical codes with which errors can be corrected easily and the detection circuit can be made simple. The following shows the merits of duplex coding.

① The minimum distance of codes is the product of two codes **correction efficiency is extremely high**

② As the two codes function as pointers to indicate the error positions, it enables correction of lost data and is effective for correcting burst error.

③ By improving the interleaving of the two codes, the codes can be used as follows, leading to higher effectiveness on the whole.
(1) The codes in the first stage are used for correction of random error and detection of burst error.
(2) The codes in the second stage are used for correction and interpolation of burst errors.

In addition, the duplex Reed Solomon codes need only be used in two tracks (tracks A and B).

CHAPTER 4. DAT MODULATION METHOD AND TRACKING

4.1. 8-10 Modulation Method and Overwriting

4.1.1 Necessity of Overwriting and Characteristic Required of Modulation method

With current analog recorders, the erasure head is located at the previous position of the recording head as shown in **Fig. 4.1** (a) to erase signals previously recorded prior to recording. This is because, with analog recording, erasure by overwriting proved insufficient.

With the DAT system, as the rotary head method is adopted, the recording track is tilted. With the current fixed erasure head method, the triangular unerased space as shown in **Fig. 4.1** (b) remains. With the DAT system, as the recording density is high and the tape speed is slow, this unerased space which could be ignored with the fixed erasure head method cannot be ignored because it lasts for more than 3 seconds. Thus digital recording is applied and the overwrite method is adopted.

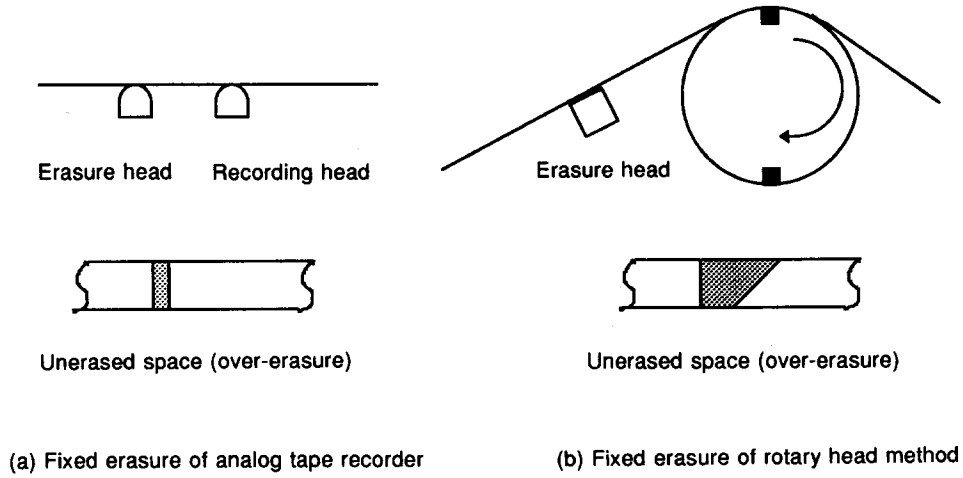


Fig. 4.1 Unerased Space by Fixed Erasure Head

With the overwrite method, an erasure head is not provided and therefore the previously written signals are erased by the signals written next. Generally, in magnetic recording in the longitudinal direction, signals with short wavelengths are recorded on the surface of the magnetic substance while signals with long wavelengths are recorded deeply as shown in **Fig. 4.2**, which makes it therefore difficult to erase signals written with long wavelengths with signals written with short wavelengths. Consequently, the modulation method suited for overwriting must have as little long waveform components as possible.

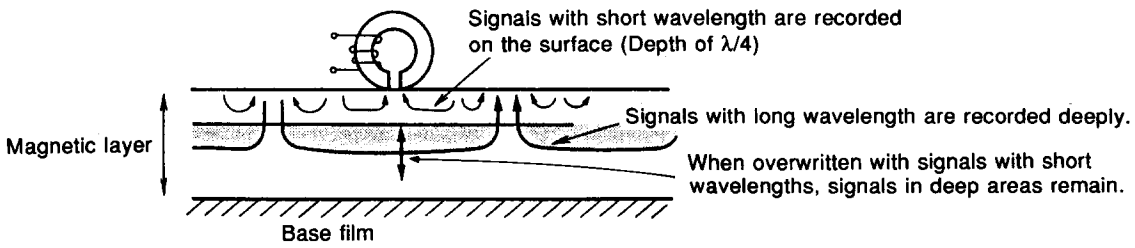


Fig. 4.2 Overwriting

4.1.2 8-10 Modulation Method

The characteristics required of the modulation method for DAT are as follows.

① No direct current components for the use of rotary transformer
② The spectrum is made up mainly of short wavelengths to enable overwriting
③ Resistant to S/N deterioration such as crosstalk and unerased areas
④ Matches well with error correction method (8-bit unit processing).

The 8-10 modulation method was adopted because it satisfied these conditions.
As its name implies, this method converts 8-bit data to 10-bit data to recording. As shown in **Fig. 4.3**, 16-bit data is divided into the **upper 8 bits** and **lower 8 bits**, and the 8-bit data is each converted to data with a few direct current components selected from the respective 10 bits. This explains why tapes are recorded with 16-bit data increased to 20-bit data.

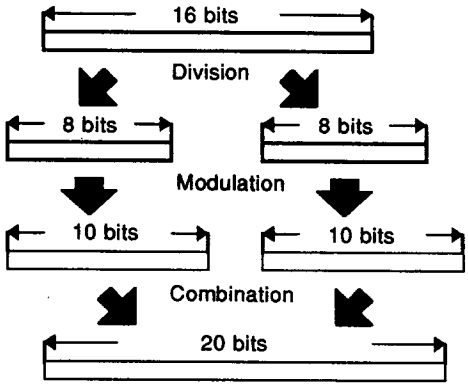


Fig. 4.3 8-10 Modulation Method

The following describes the mechanism of the 8-10 modulation method.
In the 8-10 modulation method, conversion is performed according to the NRZI (Non Return Zero Inverse) rule. NRZI, as shown in **Fig. 4.4**, inverts the current when "1" and outputs the recording current at it is when "0". As the direction inverted in is irrelevant, the magnetization pattern polarity can be from N pole to S pole or vice versa.

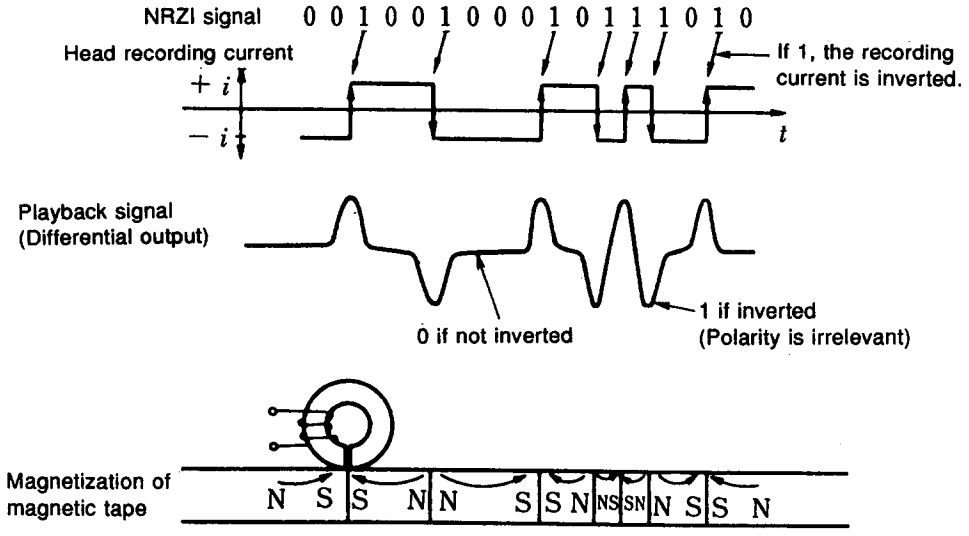


Fig. 4.4 NRZI Modulation

4.2 ATF Method

4.2.1 Outline

The ATF (Automatic Track Following) method is a technology which automatically imposes servo using the rotary head and traces the target track.

Until now, the control track method (CTL method in short) was used for the rotary head method. As shown in **Fig. 4.5**, with the CTL method, a CTL track is provided at the edges of the tape independently from the rotary head, and CTL signals are recorded with a fixed head separately from the rotary head. During playback, the signals of the CTL track are read to control the tape feed phase so that the rotary head traces the recorded track in the same way during recording. However, because it is an indirect method using the fixed head, the tracking position shifts due to the position of the fixed head and the extension and contraction of the tape, the method is not suitable for high density recording.

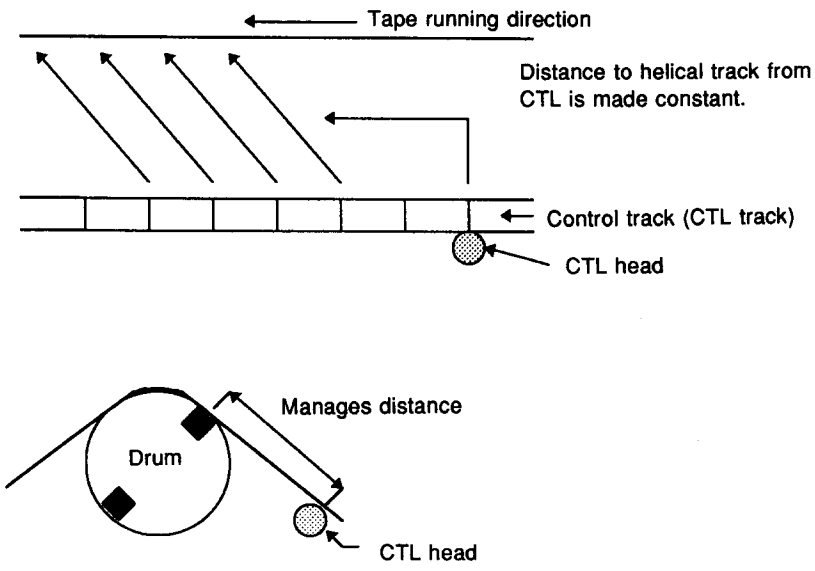


Fig. 4.5 Control Track Method

With the ATF method, signals recorded by the rotary head are recorded together with tracking signals as shown in **Fig. 4.6**, and during playback, the rotary head itself detects the tracking signal to calculate its own head position and sends the error signal to the capstan motor.
The following are the merits of the ATF method.

- As the playback head detects the error from the target track directly, it is possible to impose a stable servo regardless of mechanical changes in dimensions such as changes in temperature, with years, etc.

- As the fixed head is not necessary, the system can be made compact, leading to reduced costs.

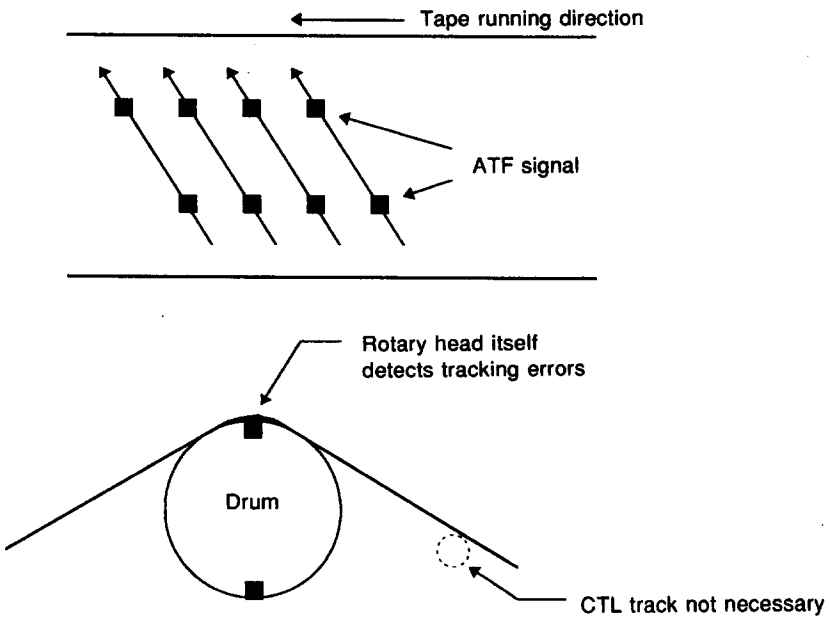


Fig. 4.6 ATF Method

Next, how tracking errors are detected is described.

4.2.2 Detection of Tracking Error

With the azimuth guard bandless recording method, the head rides onto the its own track as well as onto the adjoining tracks as shown in **Fig. 4.7**. Because only the signals of its own tracks are detected, only the signal level decreases when tracking errors occur, and therefore the direction of the deviation cannot be determined.
By detecting the signal level of adjoining tracks, the direction of deviation can be known easily just by monitoring these levels. The ATF method therefore records pilot signals for detecting tracking errors in adjoining tracks to detect the level.

If the frequency of the pilot signals is high, the output from the adjoining tracks decrease due to the azimuth effects and the characteristics of the tracking error deteriorates. While, if the frequency is low, the erasure rate deteriorates, resulting in deterioration of the overwrite characteristics. Consequently, the **130 kHz** signal is selected as the pilot signal because it has both good tracking characteristics and overwrite characteristics.

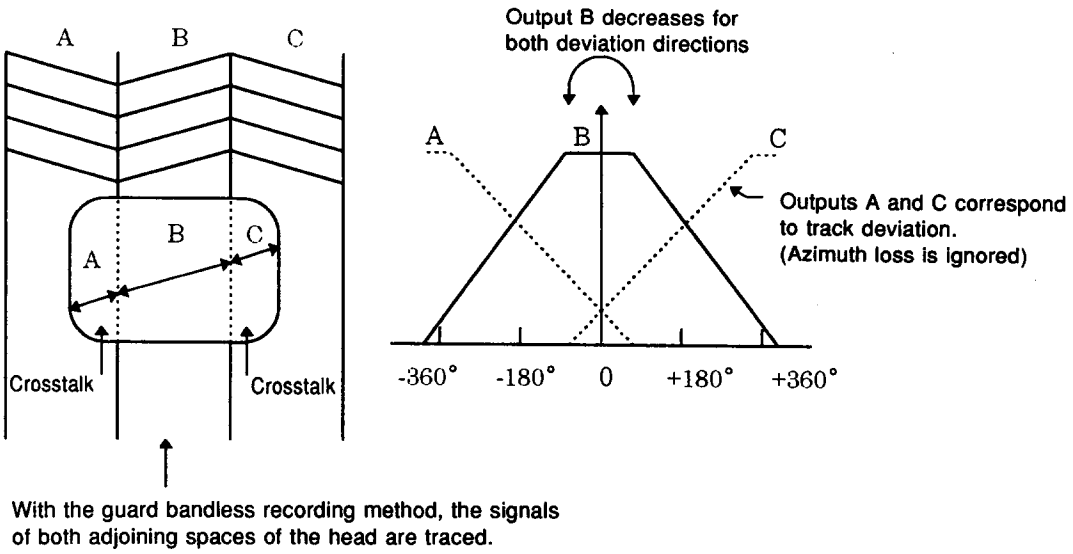


Fig. 4.7 Concept of ATF Method

4.2.3 Features of DAT ATF

The features of the ATF method are as follows.

(1) Independent areas

- Sub-code after recording, etc. is possible
  As the time-division process is performed, the reference timing is obtained by detecting the sync signal recorded on the track, providing high resistance to wow flatter and jitters.

(2) 2-point ATF

- Optimum tracking is performed for linear deviation of the track
- If one ATF signal falls off the track due to scratches and dropout of the tape, it will be covered by the other ATF signal, enabling stable tracking and the performance of the error correction method to be displayed to the full.
- Useful for improving linearity and variable speed playback

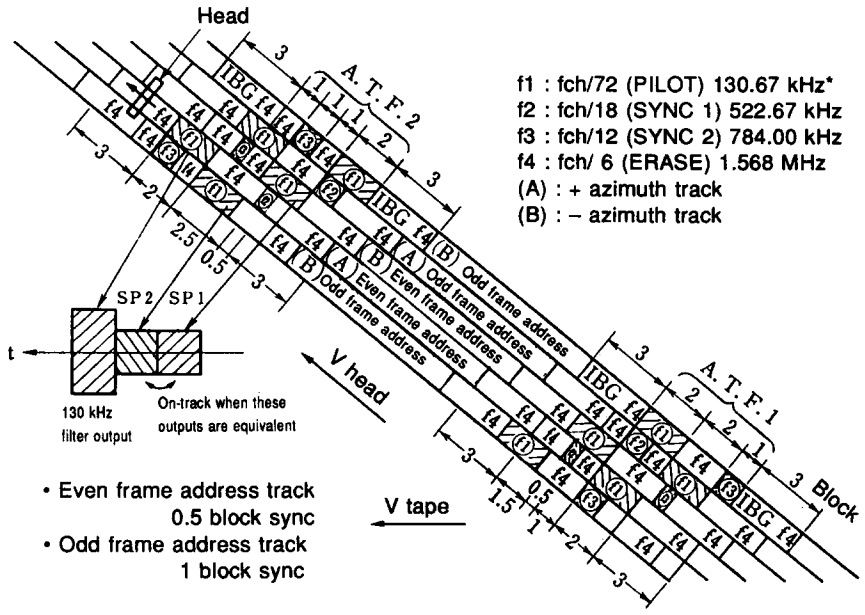
(3) Single frequency time divided pilot

- The pilot signal appears deviated time-wise from the adjoining tracks

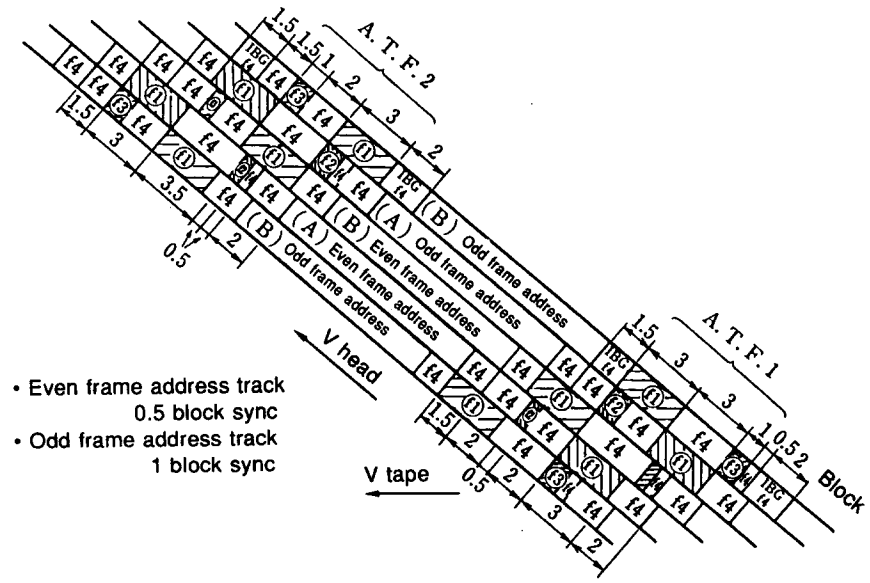
(4) 4-track completion type

- As shown in **Fig. 4.8**, four patterns, namely the pilot signal (f1), sync signals (f2 and f3), and erasure signal (f4) are repeated for every four tracks, to form a four-in-one track pattern.

f1 : Pilot signal (130 kHz)
f2 : + azimuth track (Head A) sync signal 1 (522 kHz)
f3 : – azimuth track (Head B) sync signal 2 (784 kHz)
f4 : Erasure signal (1.5 MHz)



(a) Normal track pitch



(b)Wide track pitch

Fig. 4.8 ATF Patterns

CHAPTER 5. SUB CODES

This chapter describes DAT sub codes. The volume of sub codes of the DAT is **about four times that of CDs**. A wide variety of applications can be considered, and enhancement of operations is being made so that users can record complicated sub codes with recording and playback devices by themselves.

5.1 Sub Code Format

Fig. 5.2 shows the recording format of the DAT sub codes.
As shown in **Fig. 5.1**, there are two kinds of DAT sub codes-main data area and sub data area.

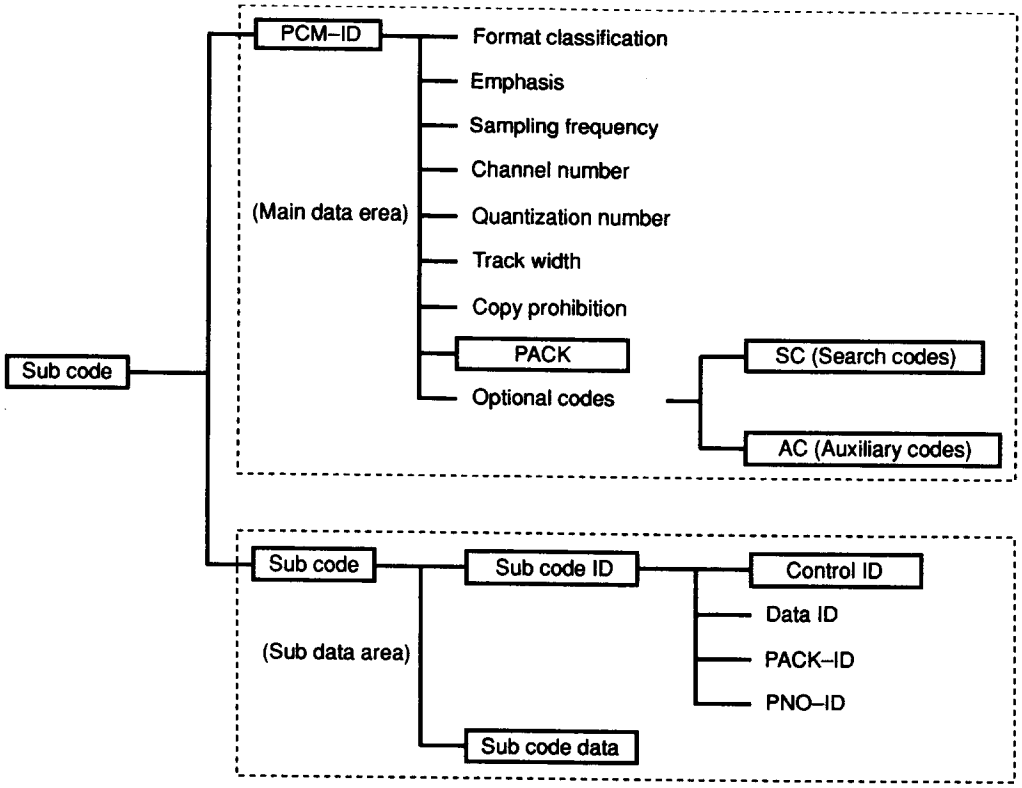


Fig. 5.1 Classification of Sub Codes

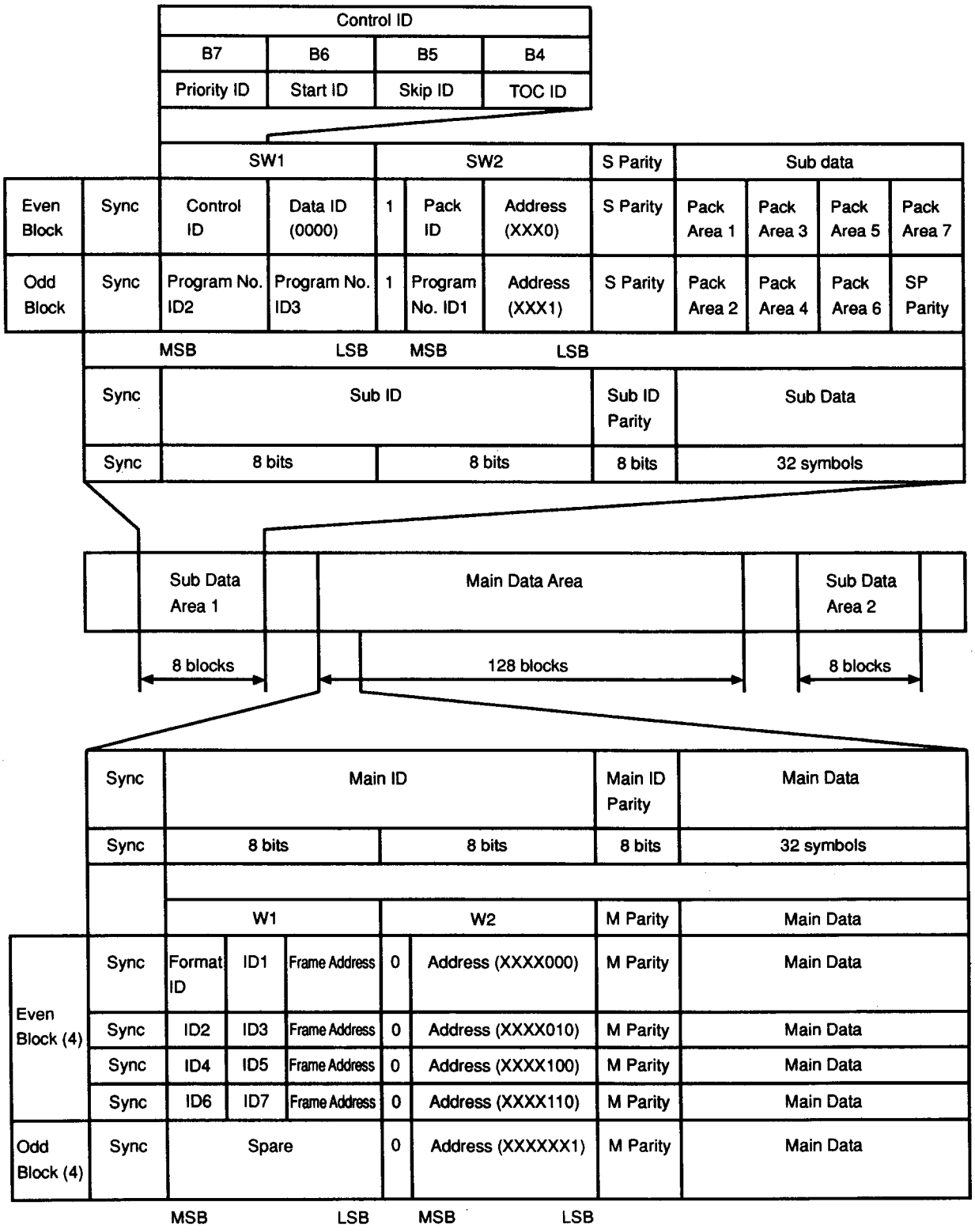


Fig. 5.2 Sub Code Recording Format

Areas that can be recorded with sub codes are the following three areas, as shown in **Fig. 5.3.**

① Main data area W1
② Empty area for main data in the main data area
③ Sub data area SW1, SW2 and sub data

Of these, only the sub data area ③ can be rewritten by after-recording.
The sub codes of the main data area and sub data area are described in the following in detail.

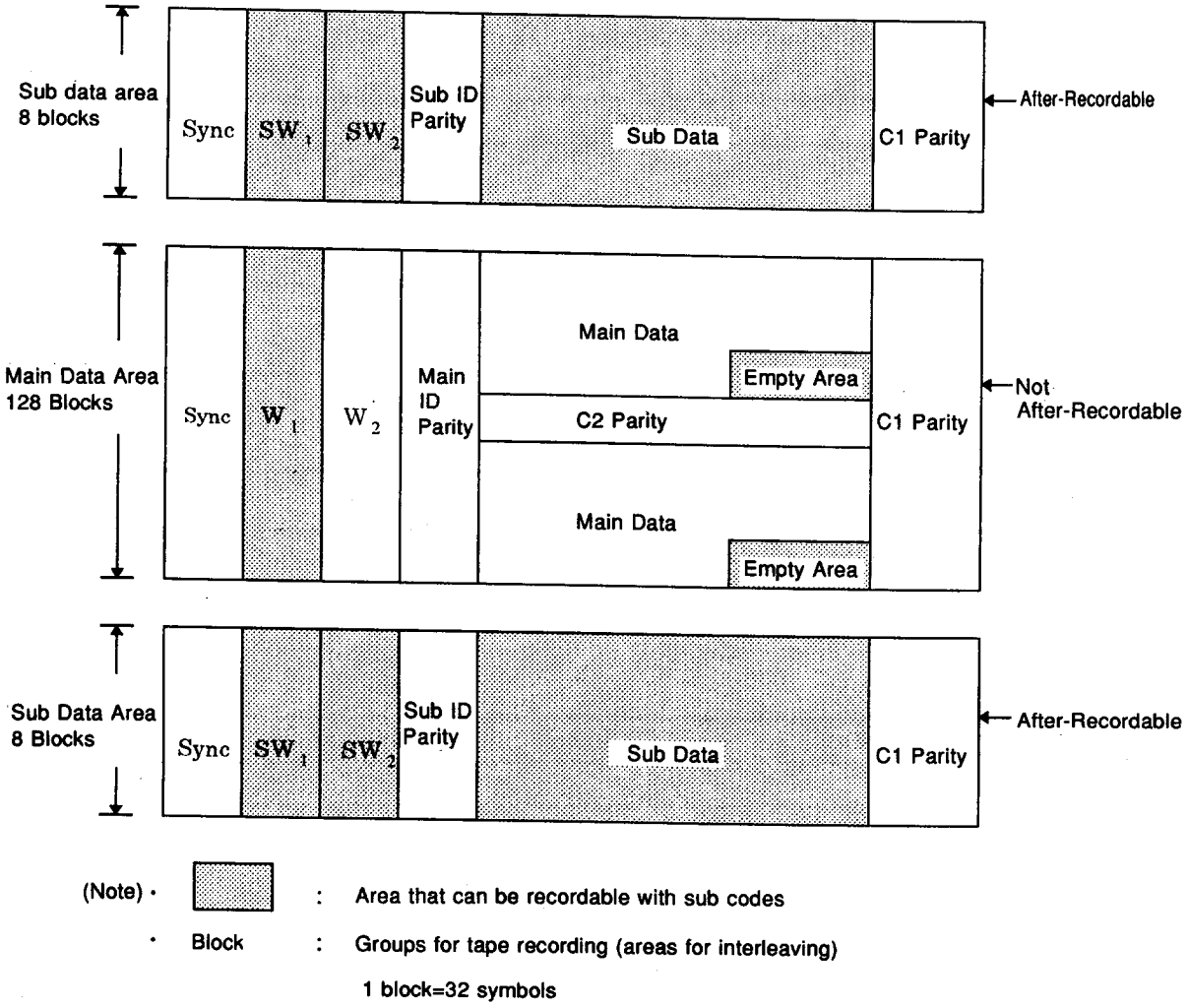


Fig. 5.3 DAT Sub Code Recordable Area

5.2 Sub Codes of Main Data Area

The sub codes in the main data are recorded in the W1 of the main ID and the empty area in the main data area. **Fig. 5.4** shows the main ID recording format.

Sync Signal	Main ID		Main ID Parity	Main Data
8 bits	8 bits	8 bits	8 bits	32 symbols

W1								W2							
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
Format ID		ID1		Frame Address				0	Address						
ID2		ID3		Frame Address				0	Address						
ID4		ID5		Frame Address				0	Address						
ID6		ID7		Frame Address				0	Address						

Fig. 5.4 Main ID Format

Of the W1 of the even address block, 4 bits are allocated to the sub codes of the FORMAT ID and ID 1 to 7, and important data is repeatedly recorded for 16 times every eight blocks. The sub codes in these blocks are recorded with data essential to playback the main data. The contents are shown in **Table 5.1**.

The 8 bits of the W1 of the odd address block are called optional codes and these are recorded with the same signals as the sub data area explained later. But because these cannot be after-recorded, the method of use is limited. As shown in **Fig. 5.1**, the optional codes are divided into search codes and auxiliary codes. The contents are shown in **Table 5.2**.

Table 5.1 ID1 to 7

ID No.	Contents (Uses)	Bit Allocation
ID1	Emphasis	B5 B4 0 0 : Not used OFF 0 1 : 50/15 μs ON
ID2	Sampling frequency	B7 B6 0 0 : 48 kHz 0 1 : 44.1 kHz 1 0 : 32 kHz
ID3	Channel no.	B5 B4 0 0 : 2 ch 0 1 : 4 ch
ID4	Quantization rule	B7 B6 0 0 : 16-bit linear 0 1 : 12-bit non-linear
ID5	Track pitch	B5 B4 0 0 : Normal track mode 0 1 : Wide track mode
ID6	Copy prohibition	B7 B6 0 0 : Permitted 1 0 : Prohibited 1 1 : Permitted for only one generation
ID7	For pack	B5 B4 Contents of pack

Table 5.2 AC (Auxiliary Codes)

AC Item	Contents
0 0 0 0	No information
0 0 0 1	Absolute time
0 0 1 0	Program time
0 0 1 1	Index time
0 1 0 0	Program no., others
0 1 0 1	Not used
0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1	Calendar information
1 0 0 0 1 0 0 1	TOC
1 0 1 0 1 0 1 1	Catalogue code
1 1 0 0 1 1 0 1 1 1 1 0	ISRC
1 1 1 1	Not used

Next, the empty area in the main data area is described.
The main data is guarded very strictly by the C1 and C2 Reed Solomon codes, as described in Chapter 4. It is an area in which data can be recorded and played back most reliably.
As this area cannot be after-recorded nor subjected to high speed search, it is suitable for recording a large volume of data such as software tapes.
For example, the empty area for the main data when the sampling frequency is 44.1 kHz is has a volume of 1.5 to 3 times the sub codes of CD.

5.3 Sub Codes of Sub Data Area

The sub codes of the sub data area has the widest application because it can be after-recorded.

Fig. 5.5 shows the format of the sub ID. In the sub data area, the SW1, SW2, and sub data area of the sub ID are used. As the sub codes in the sub data area are recorded with data required for high speed search, the sub ID has a length of 32 bits including the sync signal and parity for check. This is because during high speed search, as the head crosses the tape diagonally, and consequently some parts of the data will always be missing if it is too long, it is essential for the data to be complete in itself in small units.

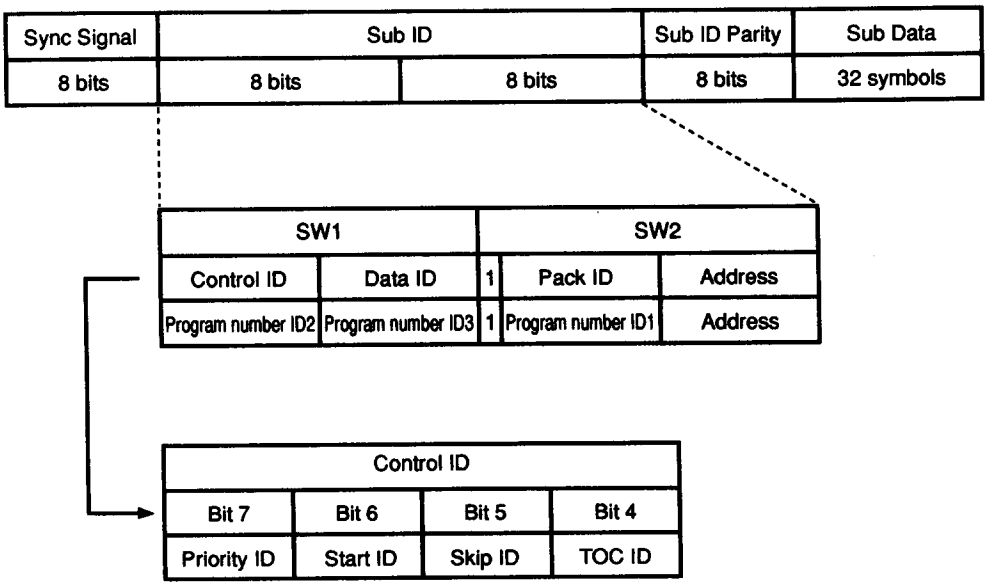


Fig. 5.5 Sub ID Format

Table 5.3 shows the relation between the IDs and their roles.
Of these IDs, the control ID is especially important. The control ID is recorded with the start ID and the shortening ID that users utilize the most frequently.

① As its name implies, the start ID is used to indicate the start of a music, and plays a major role in high speed search. As there is no way to estimate where the start ID is recorded, and as there is a need to read it steadily during high speed search, the start ID is recorded for 9 seconds (LP mode: 18 seconds).

② The shortening ID (also called skip ID) is useful for cutting the unrequired portions of the recorded tape.

Table 5.3 SUB ID

	Contents			
Data ID	Indicates how to use the sub ID, 0000 = For audio			
Control ID	B4	TOC ID		Indicates the presence/absence of TOC
	B5	Shortening ID (Skip ID)		Indicates the start of unrequired portions of tape
	B6	Start ID		Indicates the start of program
	B7	Priority ID		Indicates the priority of sub codes
Program NO. ID 1 to 3	ID1	ID2	ID3	
	0	0	0	No number
	0 to 7	0 to 9	1 to 9	Program number 1 to 799
	0	A	A	Undefined number "1010"
	0	B	B	Read-in area "1011"
	0	E	E	Read-out area "1110"
Pack ID	Indicates the pack number of the sub data area (0 to 7)			

5.4 Sub Codes of Sub Data Section

This area is imposed with the C1 Reed Solomon code completed in 2 blocks, just like the main data area. Various types of sub codes can be recorded in small units. In addition, a pack made up of 64 bits which can also be read i high speed search is used. The pack is, as shown in **Fig. 5.6**, located at seven spots covering two blocks, and will be recorded for the number defined by the pack ID.

An example is shown in **Fig. 5.7**. The pack is first made up of 4 bit (B7 to B4) items, then a 52-bit data area, and finally 8-bit parity.

	B7	B6	B5	B4	B3	B2	B1	B0
PC1	Pack item 4 bits							
PC2								
PC3								
PC4								
PC5								
PC6								
PC7								
PC8	Pack parity 8 bits							

Fig. 5.6 Pack Format

	B7	B6	B5	B4	B3	B2	B1	B0
PC1	Pack item 0	0	0	1	0	Program no. 1		
PC2	Program no. 2				Program no. 3			
PC3	Index no.							
PC4	Hours (PH)							
PC5	Minutes (PM)							
PC6	Seconds (PS)							
PC7	Frame							
PC8	Pack parity							

Fig. 5.7 Example of Pack (When pack item is 0001)

By adopting such a structure, data completed in a short block even during high speed search, enabling reading and checking of errors. Multiple recording is performed to improve precision and reliability.
By changing the 4-bit item area, the pack can be recorded with various data such as;

- Program time
- Absolute time from head of tape
- TOC

Table 5.4 shows a list of the items currently available.

Table 5.4 List of Pack Items

Pack Item	Contents
0 0 0 1	Program time
0 0 1 0	Absolute time
0 0 1 1	Running time
0 1 0 0	TOC
0 1 0 1	Calendar information
0 1 1 0	Catalogue cord
0 1 1 1	ISRC
1 0 0 0 to 1 1 1 1	Not used

CHAPTER 6. DAT CASSETTE AND TAPE

6.1 Features of DAT Cassette

The DAT cassette is a new type of cassette intended for the DAT system. It is completely different from compact cassettes and 8 mm VTR cassettes using the rotary head method.

The features of the DAT cassette are as follows.

① Flangeless cassette with external dimensions of 73x54x10.5 mm
② Continuous recording time of two hours with a standard tape
③ Completely sealed off structure with use of slider to seal off hub hole, and front cover lock mechanism
④ Hub brake mechanism linking to front cover to prevent slacking of tape.
⑤ Prism type tape end detection mechanism effectively using guide pin storage area inside cassette
⑥ Reusable tape rec-proof mechanism, and four identification holes
⑦ Loading grip for drawing in cassette

6.2 Structure of DAT Cassette

Fig. 6.1 shows the external structure of the DAT cassette and **Fig. 6.2** shows the internal structure.
The following describes the four holes for identification and one hole for rec-proof detection shown in **Table. 6.1**. These four identification holes play an enormous role in the operations of the system, and opening or closing them unintentionally may result in improper operations of the system.

Table 6.1 Purpose of Use of Hole

Hole (1)	Hole (2)	Hole (3)	Contents
0	0	0	Metal tape or equivalent/standard tape thickness
0	1	0	Metal tape or equivalent/thin tape
0	0	1	Wide track tape/standard tape thickness
0	1	1	Wide track tape/thin tape
1	X	X	Not specified (For future use)

Hole (4)	Contents
1	Prerecorded tape (Playback only tape)
0	Blank tape

Note) "1" Open, "0" Close

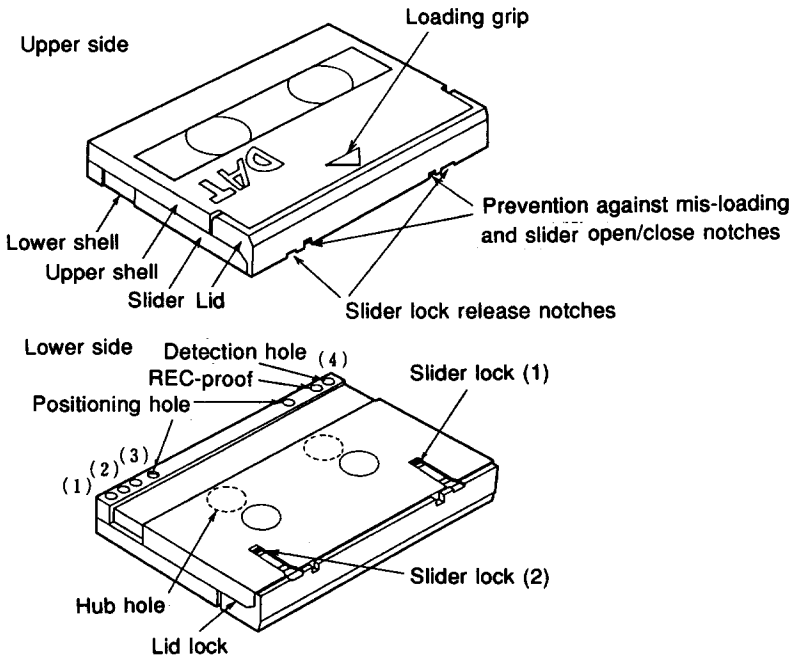


Fig. 6.1 External Structure of DAT Tape

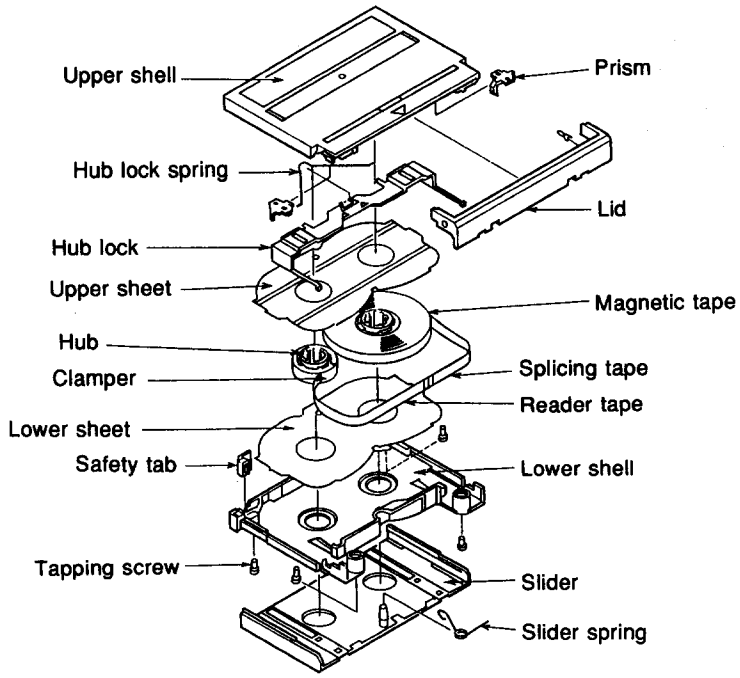


Fig. 6.2 Internal Structure of DAT Tape

The rec-proof hole can be switched with a switch as shown in **Fig. 6.3** so that it can be used over and over again.

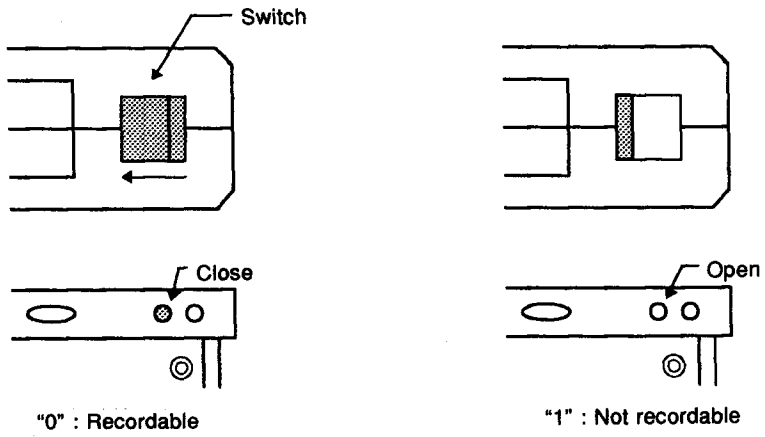


Fig. 6.3 Rec-Proof Switch

Next, the mechanism of tape end detection is described. With the DAT system, this tape end detection is performed using the optical detection method. A transparent reader tape (passes light) is attached at the start and end of the tape. The magnetic tape does not let light pass. The DAT tape is incorporated with a prism. As shown in **Fig. 6.4**, the light from the light emitting section passes through the tape at the start and end of the tape and reaches the prism for the light sensing section to detect "tape-top" or "tape-end" via the prism.

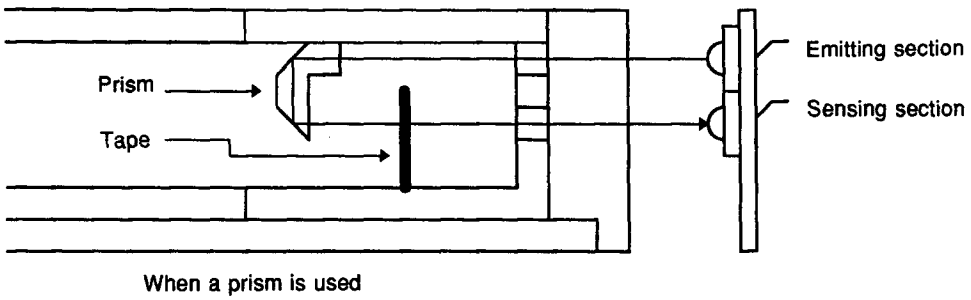


Fig. 6.4 Tape End Detection Method 1

Recently, in some models, instead of using a prism inside the tape, the light emitting section is set at the center of the mechanism section and the light sensing section is set both ends of the mechanism section as shown in **Fig. 6.5** to detect the "tape-top" and "tape-end" using the light detection method.

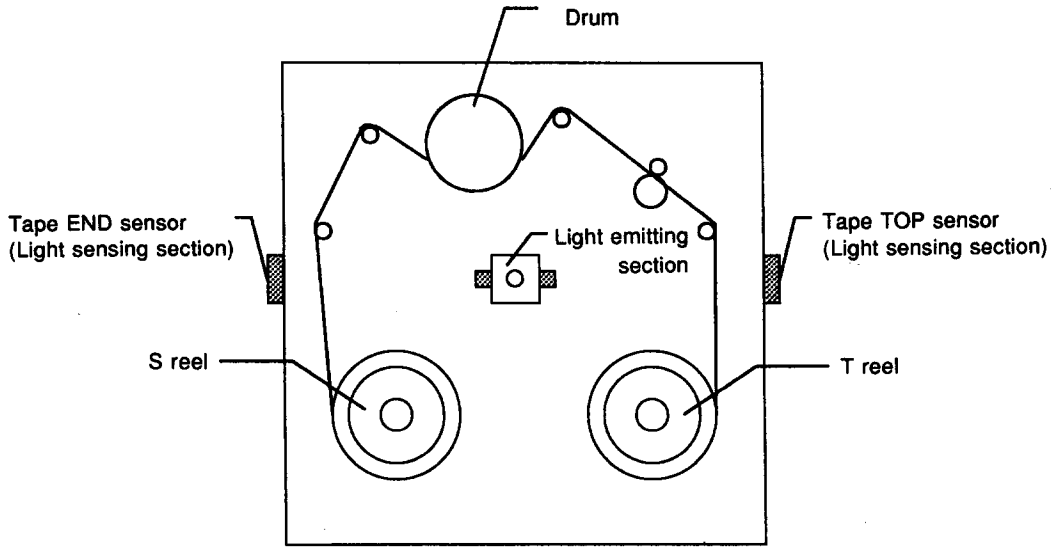


Fig. 6.5 Tape End Detection Method 2

Remarks
== DAT Cassette Tape Checking Method ==
To slide the cassette with your hand when checking the DAT cassette tape, lower the slide in the arrow direction while holding the slider locks (1), (2) with both thumbs as shown in **Fig. 6.6**.

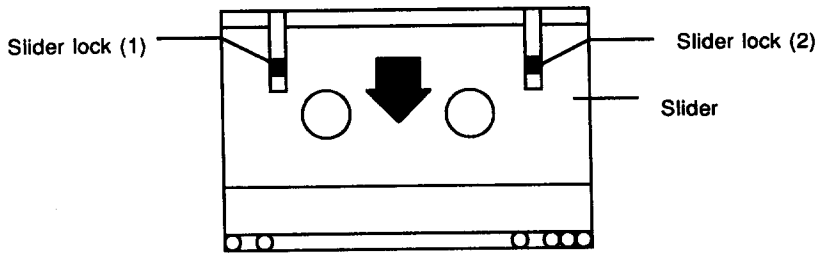


Fig. 6.6 Manual Sliding Method

CHAPTER 7. DIGITAL AUDIO INTERFACE

7.1 Digital Audio Interface

Most digital audio equipment such as CD players, BS tuners, PCM processors, DAT systems, etc. are equipped with a digital output (digital out), which cannot output nor input signals at all if the format, sampling frequency, input/output connector, etc. do not match.

For this digital signal output to be compatible, the digital audio interface standard*1 was created.

*1 : Adopts the serial transmission signal format conforming to the "digital audio interface format" of IEC958 (IEC: International Electrotechnical Commission).

7.2 Format

Fig. 7.1 shows the digital output signal format. The top part of **Fig. 7.1** shows how the transmitted signal is arranged by time. The serial-transmitted digital signals are composed of 64 bits, in which the pair of Lch and Rch 1 sampling information is called "frame".

As shown in the middle part of **Fig. 7.1**, the information of one channel is composed of half of this one frame-32 bits. The 1 sampling information of either channel is called "sub-frame" or "word". Therefore, two sub-frames of Lch and Rch form one frame.

As shown in the bottom part of **Fig. 7.1**, the first four bits of the sub-frame are the sync signal, the next four bits are spare bits, the following twenty bits form the audio data area, and the last four bits, which are four types of 1-bit codes (V, U, C, and P), are the control signal which carries signals accompanying the data such as copy prohibition and emphasis.

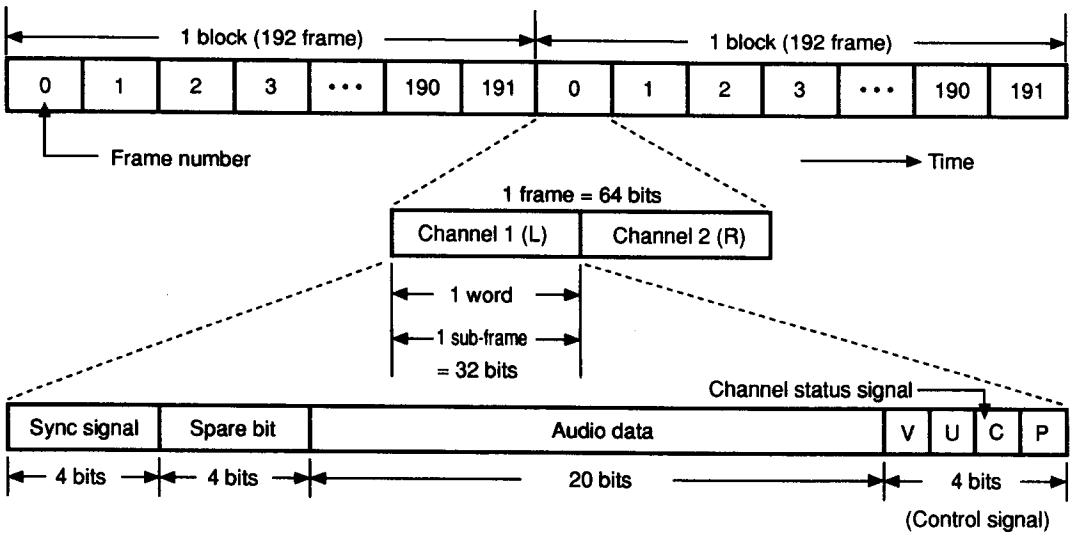


Fig. 7.1 Digital Out Signal Format

7.2.1 4 Types of Control Signal

Table 7.1 shows details of the 4 types of control signals.

Table 7.1 Details of Control Signal

	Name	Details
V	Validity	Flag which shows whether the data is effective and consequently whether it contains errors or not
U	User's bit	Used for transmitting the sub code information on each equipment
C	Channel Status	Input with control information such as the ON/OFF of emphasis and copy prohibition information
P	Parity	Used with the aim of detecting errors during transmission and keeping the polarity of the sync signal always the same

The "C" channel status signal is described below as it plays an important part in the SCMS (serial copy management system) described later.

7.2.2 Channel Status Signal

Fig. 7.2 shows the channel status signal format.
One block of the digital audio interface format signal contains, as shown in **Fig. 7.1**, 192 frames from frame 0 to frame 191. The "C" signal in each frame contains one bit each. Consequently, as shown in **Fig. 7.2**, for the channel status signal, 192 bits form one set. The details are as follows.

① Copy prohibition code is 1 bit
② Code showing ON/OFF of emphasis is 2 bits
③ Code showing type of signal source called category code is 8 bits
④ Source number is 4 bits
⑤ Code showing channel number is 4 bits
⑥ Bits showing sampling frequency is 4 bits
⑦ Code showing accuracy of transmission clock of the transmission side is 2 bits

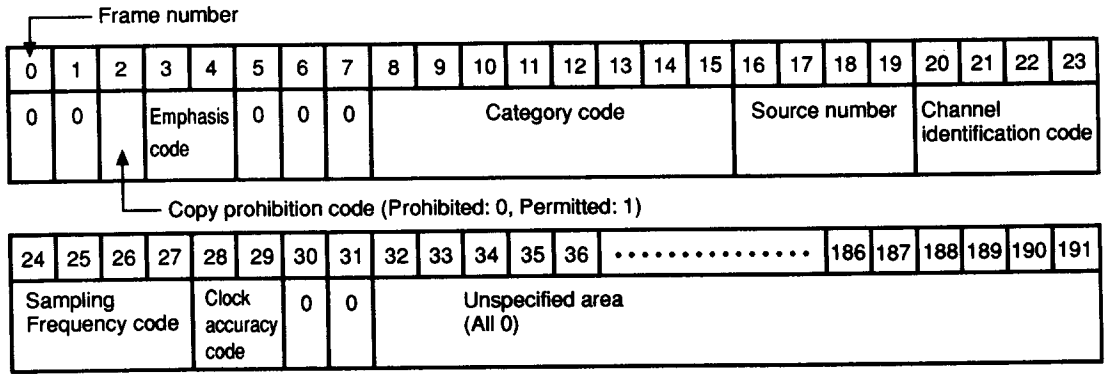


Fig. 7.2 Channel Status Signal ("C") Format

7.2.3 Category Codes

Category codes are provided for the reception side to identify what is the transmission side of the digital signal. **Table 7.2** shows the main public digital audio source category codes.

Table 7.2 Example of Consumer Use Audio Category Code

Category Name	Category Code
General	00000000
CD	10000000
PCM processor	01000000
DAT	11000000
DAT-P	11000001
MD	10010010
MD-P	10010011

Amongst these, "general" is used for sources which have no corresponding category codes, products produced before the category codes were fixed, and sources for which the presence/absence of rights information was unknown (whether can copy or not) with the analog signal originally such as signals which have passed through the AD converter.

CHAPTER 8. OUTLINE OF SCMS

The SCMS (Serial Copy Management System) is, as its name implies, a system which controls serial copy digitally by DAT.
Regarding DAT digital copy, in July 1989, a proposal for a resolution based on the agreement of those concerned was announced, and from May 1990, on receiving official notification from the Ministry of International Trade and Industry, this method was adopted for products produced thereafter.

8.1 SCMS Method in Different Uses

The following describes the different uses of the SCMS method.
(1)Digital copy from playback only MD and playback only DAT tape
Although digital outputs from CDs, playback only MDs, and playback only DAT tapes contain copy prohibition codes, only the first generation is allowed digital recording, while copy is not allowed for generations thereafter.

There is no restriction on copying of digital-recorded media with the analog input/output.

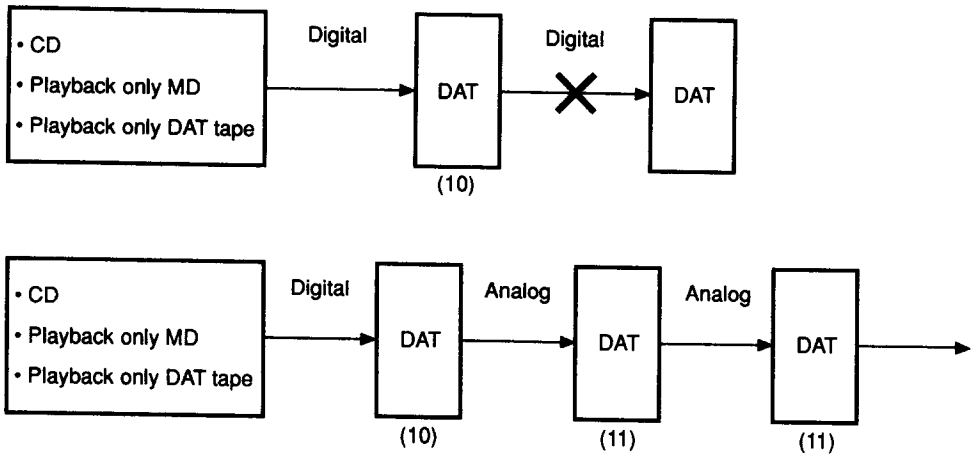


Fig. 8.1 Digital Copy from Software Tape

(2)Analog Copying
Copied tapes from analog sources are taken as DAT music tapes with copy prohibition codes, but there are no restrictions on copying using the analog input/output.

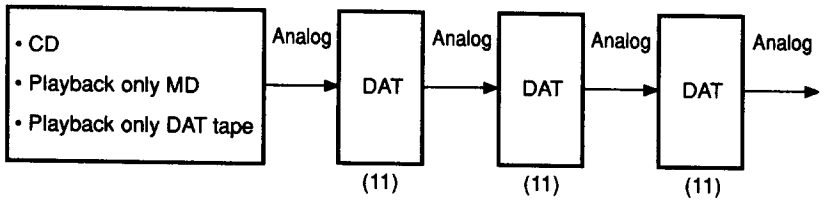


Fig. 8.2 Analog Copying from Software Tapes

3)Digital Copying from Analog Copied Tapes

The analog signal output only has an audio signal and no copy prohibition codes, etc. This input can be recorded with the DAT. But tapes recorded with this method are taken as DAT music tapes containing copy prohibition codes regardless of whether there are inputs or not, because there is no method available for identification. Consequently, digital copying from such tapes is possible, but digital copying after that is not allowed. For analog input/output, like CDs of digital source, microphones, FM tuners, analog recorders, etc. are also handled in the same way regardless of the digital sources.

This means that once a signal which has passed through an A/D converter is recorded by DAT, this copy tape will become a DAT music tape with copy prohibition codes.

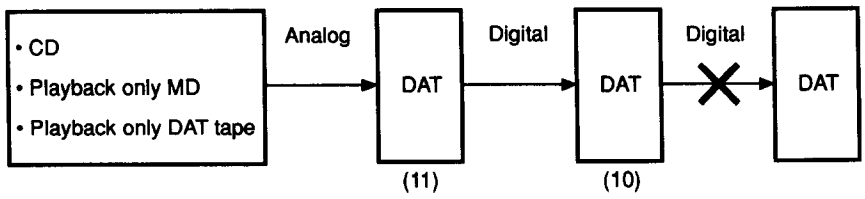


Fig. 8.3 Digital Copying from Analog Copied Tapes

(4)Digital Copying when Category Codes are "General" (BS tuners, etc.)

When category codes are "general", digital copying can be performed for the second generation as well even if the tape contains copy prohibition codes. And, even if copying is permitted, digital copying can be performed only to the second generation.

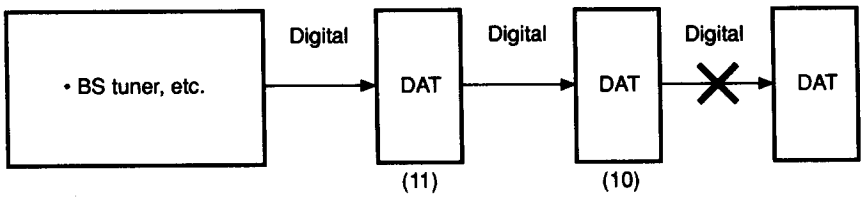


Fig. 8.4 Digital Copying when Category Codes are "General"

(Note) The ( ) in the figure indicate the ID6 bits.
00 : Digital copying permitted
10 : Digital copying prohibited
11 : Digital copying permitted only for 1st generation

8.2 Processing Routine of SCMS Method

Fig. 8.5 shows the digital copy processing routine of the SCMS method
For digital inputs, digital copy prohibition/permission and ID6 are determined by this routine. For digital copy to be permitted, ID6 must be recorded on the tape.

① First the digital input signal is checked whether the channel status bits 0 and 1 are consumer-use audio data (both bits 0 and 1 must be 0).
For commercial-use digital data, copy is prohibited.

② As there may be a possibility that new category codes will be set in the future, software tapes with category codes not existing now are taken as copy permitted software, and ID6 is set to 10 to permit digital copying.

③ In the case of "General" (00000000), a special example of category codes, ID6 is set to 11 regardless of the presence/absence of copy prohibition codes like the A/D converter output, to permit digital copying. In the BS tuner, the category code is output by "General" and corresponds to this.

④ The bit 2 and copy prohibition/permission of the channel status is checked here.
If the copy prohibition code is "permit" (bits 2 is "1"), then ID6 is set to 00. In this case, digital copying will not be restricted thereafter.

⑤ Even if the copy prohibition code is "prohibit" (bit 2 is "0"), digital copying is permitted according to the category code. These category codes include CD (10000000), DAT-P (11000001), MD-P (10010011), etc. For example, direct digital copying from CDs and the signal from the DAT digital output when ID6 is 11 are such cases. ID6 is set to 10 to permit digital copying and the code is recorded on the tape.
In the case of DAT digital output when ID6 is 10, whether digital copy is prohibited or not is determined.

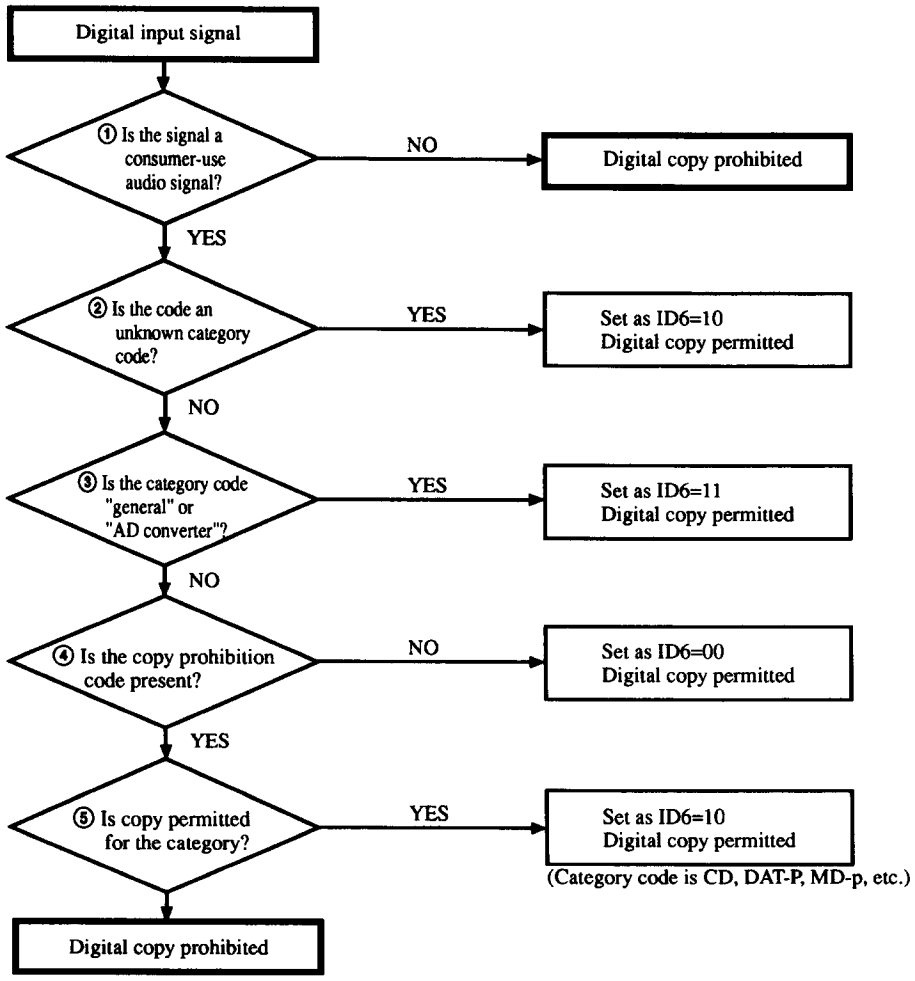


Fig. 8.5 SCMS Method Processing Routine

8.3 DAT Council Complying Products and SCMS Complying Products

There are two types of DAT products, the portable type and installed home type.
These products are also classified according to their "generation" in which the time they were sold and structure of internal circuit differ.
Table 8.1 shows the various models and their generation. The 1st generation is DAT council complying products and the 2nd generation and after is SCMS complying products.

Table 8.1 Models and Generation

	Portable	Home Type
1st Generation	TCD-D10	DTC-300ES DTC-1000ES
2nd Generation	TCD-D3	DTC-670 DTC-690 DTC-55ES/75ES/700 DTC-57ES/750 DTC-59ES DTC-60ES DTC-77ES/87ES DTC-A7 DTC-P7
3rd Generation	TCD-D7 (K) WMD-DT1*1 TCD-D8	DTC-790 DTC-2000ES DTC-A8 DTC-ZA5ES

*1: WMD-DT1 is a playback only model.

2. FUNCTIONS AND FEATURES

This unit and TCD-D7 are portable DATs using the 3rd generation signal processing LSI.
Their basic system structure and mechanisms are more or less the same, but as they use different microprocessors for their mechanism controller/servo, some functions differ as shown in **Table 2-1**. New functions such as analog recording mode whose sampling frequency is 44.1 kHz, REC MUTE function which creates mute areas during recording, and a function which sets the low power consumption mode forcibly have been added to facilitate use.
By adopting a high packing density 6-layer board and a mechanism deck which mounts a head drum with a diameter of 15mm, they have been made lightweight and compact.

Table 2-1. Main Differences in Specifications and Functions

Model	2nd Generation	3rd Generation	
	TCD-D3	TCD-D7	TCD-D8
Time of Marketing	February 1991	April 1993	October 1995
Measurements (Width/Height/Depth)mm	85.2/40/145.9 (Including battery pack)	Approx. 132.6/36.7/88.2	Approx. 132.6/36.7/88.2
Weight	Approx. 630g (Including battery pack)	Approx. 500g (Including dry batteries)	Approx. 510g (Including dry batteries)
Power Supply	ACP-D3 (Provided) DC IN 9V jack BATT pack (BP-D3)6V	AC-E60L (Sold separately) DC IN 6V jack AA battery (Four)	AC-E60D (Provided) DC IN 6V jack AA battery (Four)
Battery Duration Time (Continuous Recording)	Approx. 2 hours	Approx. 4 hours (When alkaline AA batteries are used)	Approx. 4 hours (When alkaline AA batteries are used)
Power Consumption	3.6W	1.2W	1.2W
Low Power Consumption Mode	X	Δ (*1)	O (*2)
Recording Level Adjustment	Manual only	Manual/auto (*3)	Manual/auto (*3)
44.1 kHz Analog Recording	X	X	O
REC MUTE Function	X	X	O
AVLS	X	O	O
Date Function	X	O	O
Input Terminal	Used for both line/microphone	Separate for line/microphone	Separate for line/microphone
Output Terminal	Separate for line/headphone	Used for both line/headphone	Used for both line/headphone
Gold Metal-plated Input/Output Terminals	X	X	O

*1: When stop state lasts for more than 3 minutes, the low power consumption mode is set
*2: When stop state continues for more than 3 minutes or when the HOLD switch is turned on in the stop state, the low power consumption mode is set.
*3: Can be selected between MUSIC and SPEECH

Recording mode
This unit is equipped with the 48k mode and 32k mode which records using the analog input, and 44k mode which records in the same format as CDs. When creating original CDs, DAT tapes recorded with this unit can be used as the master tape. Connecting the optional super bit mapping (SBM) adapter (SBM-1) enables high sound quality recording equivalent to 20-bit quantization. **Table 2-2** shows the recording modes of this system.

Table 2-2. Recording Modes of TCD-D8

	Sampling frequency	Quantization bit no.	Max. recording time	Input and Source
48k mode (Standard)	48 kHz	16-bit linear	120 minutes	Digital (DAT and satellite broadcast B mode)
				Analog (General source)
44k mode	44.1 kHz	16-bit linear	120 minutes	Digital (CD, MD)
				Analog (General source)
32k mode (Option 1)	32 kHz	16-bit linear	120 minutes	Digital (Satellite broadcast A mode)
32k • LP mode (Option 2)	32 kHz	12-bit non-linear	240 minutes	Digital (Satellite broadcast A mode)
				Analog (General source)

(Note) The satellite broadcast sampling frequency differs according to the mode. The A mode is 32kHz and the B mode is 48 kHz.

- For digital input, the mode is automatically selected according to the sampling frequency of the digital signal. The 32k mode can be selected from options 1 and 2.
- When performing analog recording, the 48 k mode, 44 k mode, and 32 k LP mode can be selected regardless of the input source.

Other Features

- High quality microphone recording. (Using the plug-in power method)
  Microphone sensitivity switch is selected according to sound source (HIGH/LOW)
  Two types of auto level setting mode (MUSIC and SPEECH)
- "Low power consumption mode" which prevents consumption of batteries.
  Normally, when stop state continues for more than 3 minutes, "low power consumption mode" is set. But by turning on the HOLD switch in the stop state, the "low power consumption mode" will be set forcibly to prevent battery consumption.
- Large and clear liquid crystal display with backlight.
- "Start ID function" convenient for setting the program search.
- Optical digital-connectable digital input/output terminal.
  Digital-connectable to MD deck using digital connection cable (optional, POC-DA12S), etc.
- Use of wired remote control unit (optional, RMT-D7) enables recording and playback to be performed anywhere, and as well as ID editing which sets the program search and music order, etc. to be performed.
- "REC MUTE function" which creates mute areas during recording.
- x100 speed high speed function for setting the program search.
- Date function which automatically records date (year/month/day), day, time (hour/minutes/seconds) of recording.
- "AVLS function" which controls sound pressure without sacrificing sound quality.
- "HOLD switch" which prevents incorrect operations and unnecessary battery consumption.

3. SYSTEM STRUCTURE

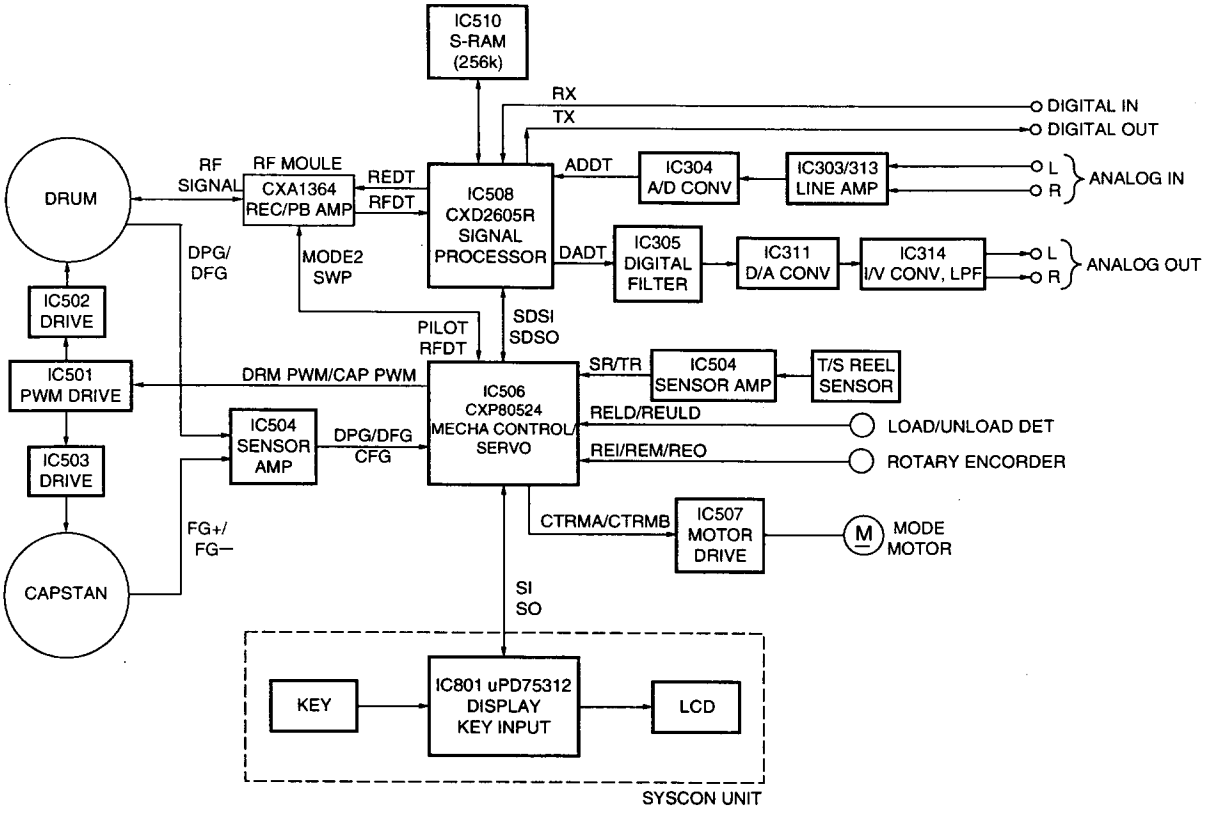


Fig. 3-1. General Structure of System

As shown in **Fig. 3-1**, the digital audio signal processing system of this system is composed mainly of the 3rd generation LSI (CXD2605R) while its servo and system control system is composed mainly of the CXP80524. The 2nd generation LSI (CXD2601AQ) consisted of most of the digital signal processing circuits required for recording and playback, digital I/O signal processing circuits, semi-NT (non tracking) demodulation processing circuits used for playing back in the LP mode, etc. The CXD2605R consists of all of these as well as a peak level meter, a function which detects sub-codes, between-musics information on the digital interface when recording from CDs, and other new functions. A x64 oversampling 1-bit A/D converter incorporating a digital filter, and a x8 oversampling dual 18-bit D/A converter are also used.

The CXP80524 is composed of a system control function which controls the whole system, a servo circuit which controls the drum, capstan, and reel servo with the software, etc. For the detection of key inputs, a display controller, a built-in drive circuit for this controller, and a display microprocessor μPD75312 with a clock function are used. For waveform-shaping of the reel FG, capstan FG, and drum FG/PG, a on-chip sensor amplifier MM1138XQ is used. This system does not have a power switch. In the use of dry batteries, unwanted battery consumption is prevented with the low power consumption mode in which only the clock function of the display microprocessor μPD75312 operates when the stop state is set for more than 3 minutes continuously or when the HOLD switch is turned on.

3-1 Microprocessor Interface

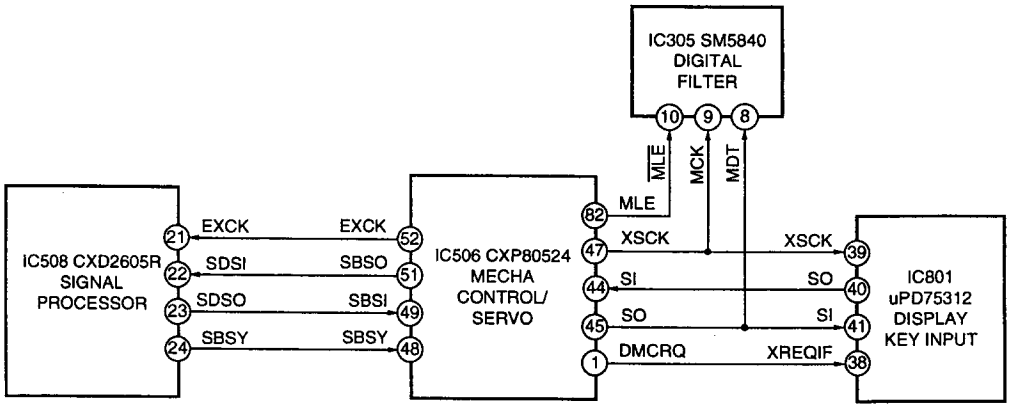


Fig. 3-2. Connection of Microprocessor Interface Signals

Fig. 3-2 shows the connection of the microprocessor interface signals between the mechanism control/servo microprocessor CXP80524 (IC506), signal processing CXD2605R (IC508), and display microprocessor μPD75312 (IC801).
The whole system is controlled by the mechanism control/servo microprocessor CXP80524. With the signal processing CXD2605R, the following information is transmitted and received according to the serial data (SDS1, SDS0) which matches the timing with the data transfer clock (EXCK) and data transfer sync signal (SBSY).

- Mode information such as recording/playback, analog IN/digital IN, etc.
- Digital audio interface data such as category code, emphasis, between-musics information from CDs
- Main-ID, Sub-ID, flag
- Control information such as sampling frequency settings, etc.
- Sub-data (PACK data)

On the other hand, with the display microprocessor μPD75312, information such as level meter display, key inputs, calendar (year/month/day, hour/minute/second) is transmitted and received according to the serial data (SI, SO) synchronized with the serial clock (XSCK), according to the serial communication request signal (DMCRQ). For the digital filter SM5840 (IC305), deemphasis ON/OFF and setting of filter coefficient are performed according to the mode set latch enable signal (MLE) and data (MDT) which matches the timing with the mode set clock (MCK).

4. POWER SUPPLY CIRCUIT

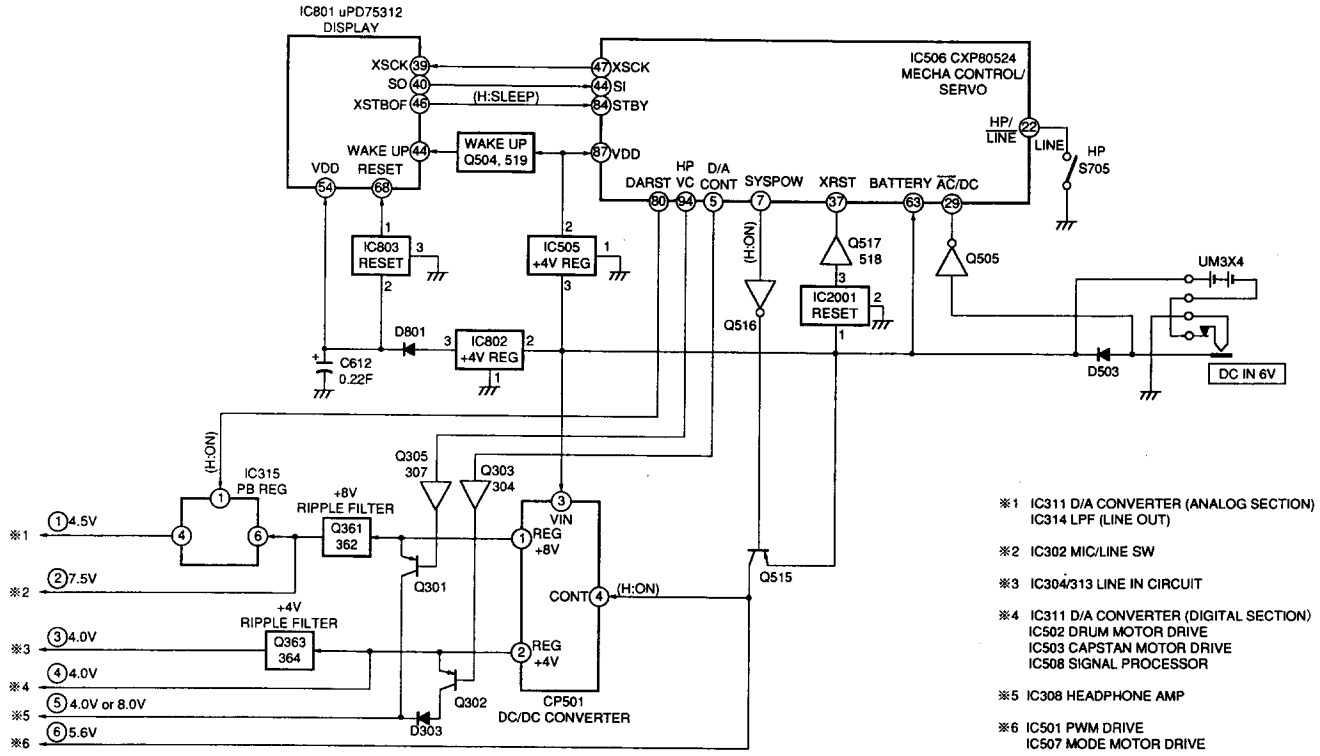


Fig. 4-1 Power Supply Circuit Block Diagram

4-1 Outline of Operations

Fig. 4-1 shows a block diagram of the power supply circuit.
Power (6V) is supplied from the AC adapter or battery to Pin ⑰ (VDD) for the mechanism controller/servo CXP80524 (IC506) via the 4V REG (IC505), to Pin ⑭ (VDD) for the display microprocessor μPD75312 (IC801) via the +4V REG (IC802) and D801, and to Pin ③ (VIN) for the DC/DC converter (CP501).
The power supply line of the display microprocessor is connected to a super capacitor 0.22F (C612) for backup because of the clock function incorporated. This ensures that the clock functions is maintained for about 1 hour when no power is supplied (i.e. when replacing batteries, etc.).
Pin ⑬ (BATTERY) of the mechanism controller/servo is an analog input. It monitors the input voltage when batteries are used and displays the power remaining in the battery on the LCD according to how much the battery has worn out.
Pin ㉙ (AC/DC) determines whether the power is supplied from the battery or AC adapter according to the power detection input. "H" is input when the power is supplied from the battery and "L" is input when power is supplied from the AC adapter.
As this system does not have a power switch, battery consumption is prevented with the low power consumption mode in which only the clock function operates when the stop state is set for more than 3 minutes continuously or when the HOLD switch is turned on.
The display microprocessor performs shift to this mode and control of restart up (WAKE UP:For details, refer to 4-4. Low Power Consumption Mode and WAKE UP.). In the low power consumption mode, it sets the sleep output of Pin ㊻ (XSTBOF) to "H" to switch the mode in the mechanism controller/servo IC.
After this, the system power control output of Pin ⑦ (SYSPOW) of the mechanism controller/servo becomes "L", Q515 connected to it turns off, and the operations of the DC/DC converter stop. As a result, the power supplied to each section also stops.

4-2 Voltage Switching of Headphone Amplifier

As shown in the figure, power ① 4.5V to ⑥ 5.6V are supplied to the respective circuits. Of these ⑤ 4V or 8V is supplied to the headphone amplifier (IC308). But according to the mode of the PHONES/LINE selection switch (S705), Pin ㉔ (HPVC) of the mechanism controller/servo outputs "L" when LINE is selected and "H" when headphone is selected to switch the Q301 connected to the REG+8V line.
As a result, as shown in **Table 4-2**, to improve the dynamic range, when headphone is selected, Q301 turns off and 4V is supplied to the headphone amplifier, and when LINE is selected, Q301 turns on so that a 8.2 dBs output can be obtained at the LINE OUT terminal on a full-scale and 8V driving is performed.
Low power consumption is implemented for the power supplied to each section in the same way as the low power consumption mode by controlling Q301, Q302, IC315, etc. as shown in the table according to the control output from the mechanism controller/servo.
The D/A converter (IC311) power uses different voltages at the analog section (4.5V) and digital section (4V). If the analog section is driven at the same voltage as the digital section (4V), the prescribed characteristics cannot be obtained. For this reason, characteristics are improved by driving on 4.5V only at the analog section.

Table 4-1. Mecanism Control/Servo (IC506) Output

Pin	㉓ DARST	㉔ HPVC	⑤ D/A CONT
"L"	Not connected	When LINE is selected	When Headphone/LINE is connected
"H"	When Headphone/LINE is connected	When Headphone is selected (When not connected)	Not connected

Table 4-2. Power Supply to Headphone Amplifier

	IC315 (4.5V)	O301 (8V)	Q302 (4V)	Remarks
When headphone is selected	ON	OFF	ON	4V is supplied to the headphone amplifier (IC308)
When LINE is selected	ON	ON	ON	8V is supplied to the headphone amplifier (IC308)
Not connected	OFF	OFF	OFF	The headphone amplifier (IC308) does not operate as no power is supplied.

4-3. DC/DC Converter (CP501)

Fig. 4-2 shows the internal circuit of the DC/DC converter (CP501).
When Pin ④ (CONT) of the DC/DC converter becomes "H" according to the system power on signal from Pin ⑦ (SYSPOW) of the system controller/servo (IC506), the IC1 oscillator oscillates at about 300 kHz and the internal circuit starts operating.
Q1 to Q4 perform switching operations. +4V is supplied from Pin ② and +8V from Pin ① to the respective circuits by performing smoothing with the capacitor connected externally.

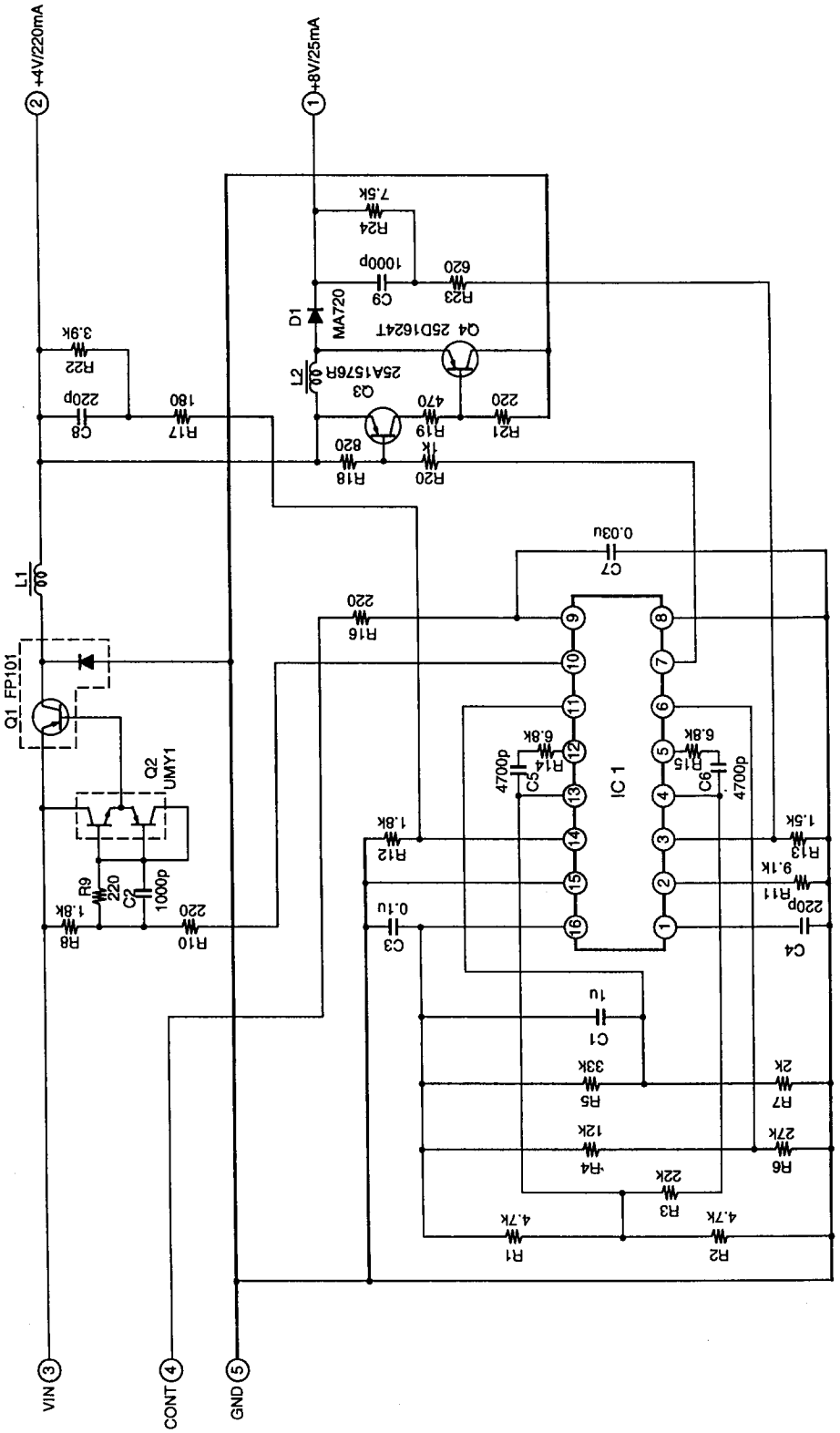


Fig. 4-2 DC/DC Converter Internal Circuit

4-4 Low Power Consumption Mode and WAKE UP

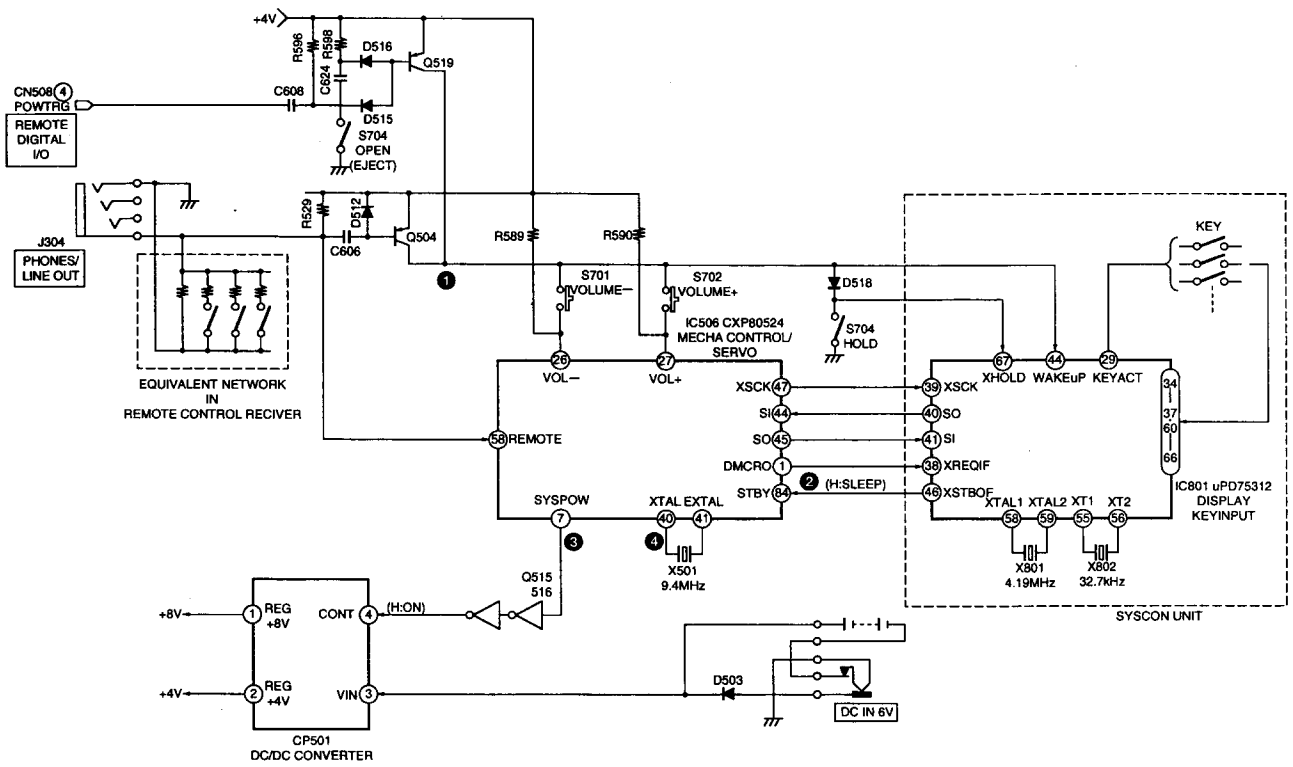


Fig. 4-3. WAKE UP Circuit

Fig. 4-3 shows the block diagram of the circuit related to WAKE UP operations.
As this system does not have a power switch, battery consumption is prevented with the low power consumption mode in which only the clock function operates when the stop state is set for more than 3 minutes continuously or when the HOLD switch (S704) is turned on.

Table 4-3. Clock Mode and Power Consumption

	IC506	System Control Unit Internal Part		Current Consumption
	X501 (9.4M)	X801 (4.19M)	X802 (32.7k)	
Power On Mode	O	O	O	Approx. 200 mA (†)
Low Power Consumption Mode	X	X	O	Approx. 200 μA

[O: Oscillation, X: Oscillation stops, †: STOP state]

As shown in **Table 4-3**, in this mode, the master clock X501 (9.4 MHz) of the mechanism controller/servo (IC506) and the master clock X801 (4.19 MHz) of the display microprocessor inside the system unit stop to set the standby state where only the reference clock X802 (32.7 kHz) of the clock operates to reduce power consumption.
In the normal power on mode, all of these clocks operate. In the STOP state, current consumption is about 200 mA.
The circuit which restarts the normal power on mode from this mode is the WAKE UP circuit. It starts operating when the following are performed, and then the whole system starts operating.

- When the headphone plug is inserted in the PHONES/LINE OUT terminal (J304).
- When the remote control unit button of the stereo ear receiver (MDR-ED7) is pressed.
- When the OPEN (EJECT) button is pressed.
- When a button on the panel of the system is pressed.
- When the volume UP or DOWN button is pressed.

Circuit Operations

As shown in **Fig. 4.4**, in the low power consumption mode, Pin ㊹ (STBY) of the mechanism controller/servo (IC506) is set to "H", Pin ⑦ (SYSPOW) is set to "L", and Pin ㊵ (XTAL) is set to "H" in the oscillation stop state.

When one of the above is performed in this state, Pin ㊹ (WAKE UP) of the display microprocessor inside the system control unit is input with the trigger pulse shown at ❶ of **Fig. 4.4**. As a result, X801 (4.19 MHz) starts oscillating, and at this timing, "L" is output from Pin ㊻ (XSTBOF) of the timing display microprocessor to the mechanism controller/servo. The X501 (9.4 MHz) of the mechanism controller/servo also starts oscillating, after which "H" is output from Pin ⑦ (SYSPOW), the DC/DC converter (CP501) starts operating to supply power to each section.

The LCD display changes from the clock display to normal displays such as counter, etc. at the same timing as the start up of the display microprocessor.

In the use of batteries, the mode is shifted to the low power consumption mode immediately after when the HOLD switch (S704) is turned on. When the STOP state continues for more than three minutes, immediately after this, "H" is output from Pin ㊻ (XSTBOF) of the display microprocessor, the oscillation of X801 (4.19 MHz) stops.

As a result, the output of Pin ⑦ (SYSPOW) of the mechanism controller/servo changes to "L", the DC/DC converter stops operating, and the oscillation of the master clock X501 (9.4 MHz) is also stopped at the same timing. If the tape is being loaded, the mode is shifted to the low power consumption mode after unloading is completed.

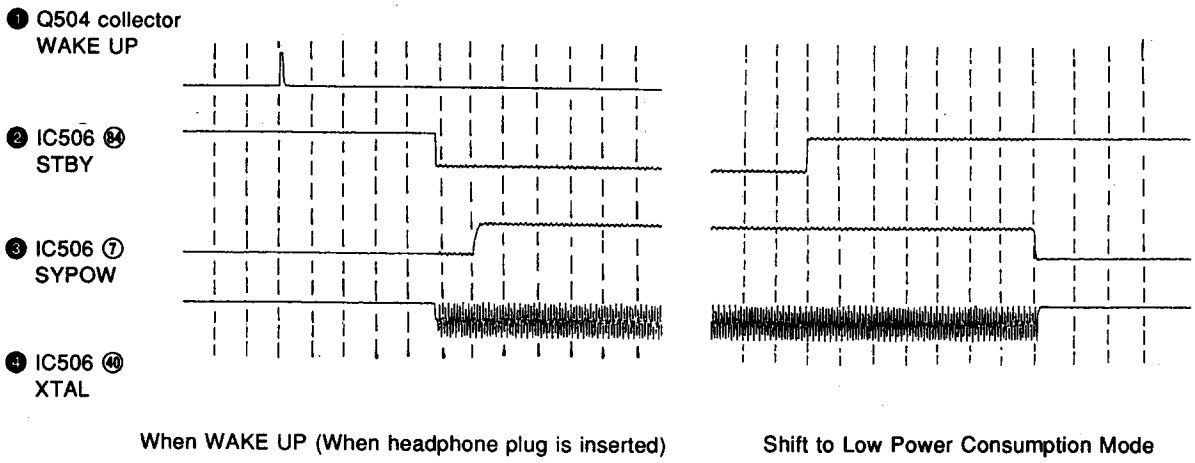


Fig. 4.4 Timing of WAKE UP and Low Power Consumption Mode (50 ms/div)

5. SIGNAL CIRCUIT

5-1 Signal Processing LSI (CXD2605R)

The CXD2605R is a 3rd generation LSI capable of performing the recording and playback signal processing of the R-DAT system on a single chip. Its functions are as follows.

- Modulation of recording signal
- Demodulation of playback signal (With use of digital PLL)
- Error correction coding processing (Generation of parity, error detection and correction)
- Microprocessor interface (Sub-code processing, system control)
- A/D, D/A interface (Includes interpolation and muting, etc.)
- Digital interface
- RAM control
- Fs system clock generation
- Peak level meter
- Error count function
- Between-musics detection function during digital recording from CDs

As shown in the block diagram in **Fig. 5-1**, the CXD2605R is divided mainly into nine blocks. The main functions of these blocks are as follows.

① DPLL (digital PLL) block
Extracts playback clocks from playback RF signals and synchronizes with playback data

② PB (playback) block
SYNC detection, 10 → 8 demodulation, demodulation and checking of playback data

③ REC (recording) block
8 → 10 modulation, generation of recording data, and generation of record control signal

④ ECC (error correction) block
Generation of C1 and C2 parities during recording, C1 and C2 error detection and correction during playback

⑤ SUB I/O (microprocessor interface) block
Interface with microprocessor such as transfer, processing of various control information and sub-code data, etc.

⑥ AD/DA I/F (AD and DA interface) block
Generation of interleave and de-interleave addresses and reference processing timings, and interface with AD and DA systems

⑦ DI/O (digital interface) block
Modulation and demodulation of digital audio interface format signals Tx and Rx and Fs system clock generation

⑧ RAM I/F (RAM interface) block
Generation of RAM interface signal such as address, etc.

⑨ PLM (peak level meter) block
Detection of peak level within a certain time

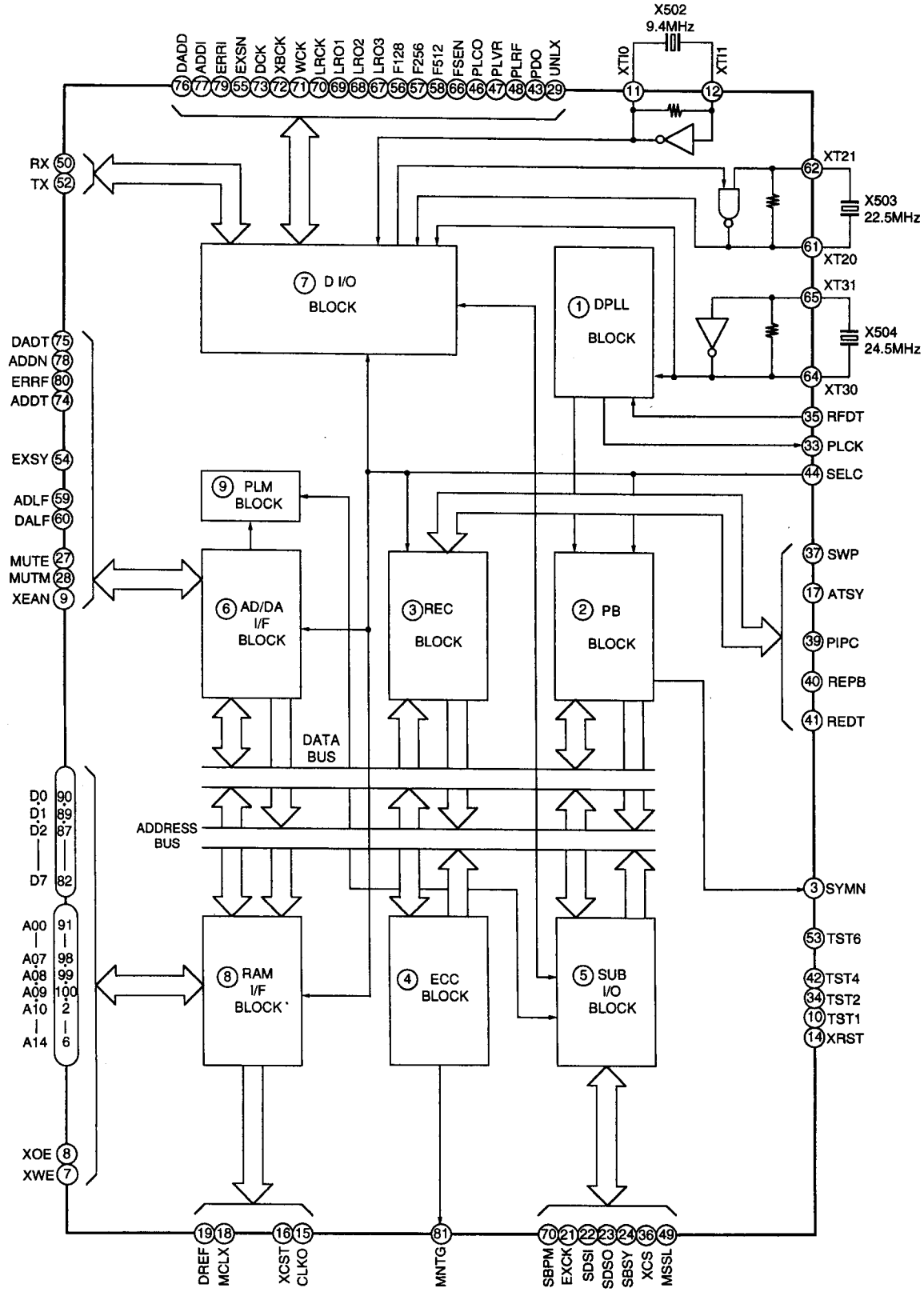


Fig. 5-1. Internal Block Diagram of CXD2605R

Pin Functions

• Signal Processor (CXD2605R)

Pin No.	Pin Name	I/O	Function
1	VDD	—	+5V
2	A10	O	External RAM address output
3	A11	O	External RAM address output
4	A12	O	External RAM address output
5	A13	O	External RAM address output
6	A14	O	External RAM address output
7	XWE	O	External RAM write enable signal output
8	XOE	O	External RAM output enable signal output
9	XEAN	O	External addressing enable signal output
10	TST1	I	Test input. Fixed at "L"
11	XT1O	O	Crystal oscillation circuit 1 output
12	XT1I	I	Crystal oscillation circuit 1 input
13	Vss	—	GND
14	XRST	I	Reset input. Reset at "L"
15	CLKO	O	System clock output
16	XCST	O	Not used
17	ATSY	I	ATF sync signal input
18	MCLK	O	Channel clock (fch) output
19	DREF	O	Duty 50 signal output in SBSY period
20	SBPM	O	Signal output monitoring data transfer to microprocessor when control byte (1) bit 1 = "L" ("L": Transfer can be performed) "H": F256 clock output by RX-PLL
21	EXCK	I	Clock input for transferring data to microprocessor
22	SDSI	I	Input of serial data from microprocessor
23	SDSO	O	Output of serial data to microprocessor
24	SBSY	O	Output of frame sync signal for transferring data to microprocessor
25	COPY	O	Not used
26	EMP	O	Not used
27	MUTE	I	Mutes when mute input is "H". REC monitor sound not muted
28	MUTM	O	Indicates mute state when mute monitor is "H"
29	UNLK	O	Indicates lock state when RXPLL lock monitor signal output is "L"
30	ERMN	I	Not used
31	SYMN	O	Output of RF C1 check results monitor signal
32	CHER	I	Not used
33	PLCK	O	Outputs RFPLL clock when control byte (1) bit 1="L" and outputs F128 clock by RX-PLL when "H"
34	TST2	I	Test pin. Fixed at "L"
35	RFDT	I	Playback RF signal input
36	XCS	I	Data can be transferred when chip select input for transferring data to microprocessor is "L".
37	SWP	I	A track when RF switching pulse is "L", B track when "H".
38	Vss	—	GND
39	PIPC	O	Outputs pilot signal when recording signal ATF pilot signal/identification signal output is "H"
40	REPB	O	REC state when REC/PB identification signal output is "H"

Pin No.	Pin Name	I/O	Function
41	REDT	O	Recording signal output
42	TST4	I	Test pin. Fixed at "L"
43	PDO	O	RXPLL phase comparator output
44	AMPI	I	Not used
45	AMPO	O	Not used
46	PLCO	I	RXPLL external VCO clock input (512 fs reference)
47	PLVR	O	RXPLL phase comparison signal output (2 fs made from PLL clock)
48	PLRF	O	RXPLL phase comparison signal output (RX SYNC detection signal 2fs)
49	MSSL	I	Master is selected when master mode/slave mode select is "H"
50	RX	I	Digital interface signal input
51	VDD	—	+5V
52	TX	O	Digital interface signal output
53	AUDR	I	Not used
54	EXSY	I/O	External sync signal input/output. Normally connected to EXSN
55	EXSN	I/O	EXternal sync signal input/output. Normally connected to EXSY.
56	F128	I/O	128 fs signal input/output
57	F256	O	256 fs signal output
58	F512	O	512 fs signal output
59	ADLF	I	LSB first is selected when ADDT, ADD1, ADDN serial data LSB/MSB first select input is "H"
60	DALF	I	LSB first is selected when DADT, DAD0 serial data LSB/MSB first select input is "H"
61	XT2O	O	Crystal oscillation circuit 2 output
62	XT2I	I	crystal oscillation circuit 2 input
63	Vss	—	GND
64	XT3O	O	Crystal oscillation circuit 3 output
65	XT3I	I	Crystal oscillation circuit 3 input
66	FSEN	I	Output when F128, BCK, LRCK input/output select input is "H"
67	LR03	O	LR02 inversion signal
68	LR02	O	Outputs LRCK 16BCK delay signal when control byte (1) bit 1 is "L" and outputs LRCK clock output by RX-PLL when "H"
69	LR01	O	LRCK 15BCK delay signal
70	LRCK	I/O	fs signal input/output
71	WCK	O	2fs signal output
72	XBCK	O	BCK inversion signal output
73	BCK	I/O	64 fs signal input/output
74	ADDT	I	AD serial data input
75	DADT	O	DA serial data output
76	DADO	I	Digital out audio data input (Normally connected to DADT)
77	ADDI	O	Digital in audio data output
78	ADDN	I	Digital in audio data input (Normally connected to ADDI)
79	ERRI	I	Digital out validity flag data input (Normally connected to ERRF)
80	ERRF	O	Interpolation data is selected when DADT data interpolation data/identification signal output is "H"

Pin No.	Pin Name	I/O	Function
81	MNTG	O	Indicates that error correction state monitor data is being output to D7 to D0 when "H"
82	D7	I/O	External RAM data input/output (MSB)
83	D6	I/O	External RAM data input/output
84	D5	I/O	External RAM data input/output
85	D4	I/O	External RAM data input/output
86	D3	I/O	External RAM data input/output
87	D2	I/O	External RAM data input/output
88	Vss	—	GND
89	D1	I/O	External RAM data input/output
90	D0	I/O	External RAM data input/output (LSB)
91	A00	O	External RAM address output
92	A01	O	External RAM address output
93	A02	O	External RAM address output
94	A03	O	External RAM address output
95	A04	O	External RAM address output
96	A05	O	External RAM address output
97	A06	O	External RAM address output
98	A07	O	External RAM address output
99	A08	O	External RAM address output
100	A09	O	External RAM address output

Digital PLL Circuit (Reference)

The signal processing LSI (CXD2605R) is provided with a digital PLL (DPLL) for extracting playback clocks from playback RF signals and performing synchronization, and digital IN PLL which generates Fs system clocks from digital audio interface format signals input to the digital IN. The digital IN PLL has both the analog PLL and digital PLL modes, but in this system, the digital PLL (DPLL) is used.

The PLL detects the phase difference between the output and input signals of the local oscillator in the circuit, and controls so that the frequency and phase of the local oscillator match those of the input signal using the feedback loop, to eliminate noises in the input signal and extract reference clocks from the input signal.
The PLL circuit can broadly be divided into the analog PLL and digital PLL. The basic structure of the analog PLL is shown in **Fig. 5-2**. The phase comparator is used to compare the input signal and output signal of the voltage controlled oscillator (VCO).
If there is phase difference between the input signal and VCO output signal, a phase difference signal corresponding to the phase difference will be generated. This signal is input to the VCO through the loop filter composed of the low pass filter. When the output voltage of the phase comparator changes according to the phase difference oscillated at the frequency corresponding to the input voltage, the VCO increases and decreases the frequency of the oscillator for the corresponding amount. The output of the phase comparator shows the phase difference of the two input signals, and the VCO output is input to the phase comparator at the same time it is output. The loop filter determines the response characteristic of the circuit and eliminates unwanted noises and harmonic components in the signal. The PLL circuit operates constantly to follow the input signal by the operation of this feedback loop.

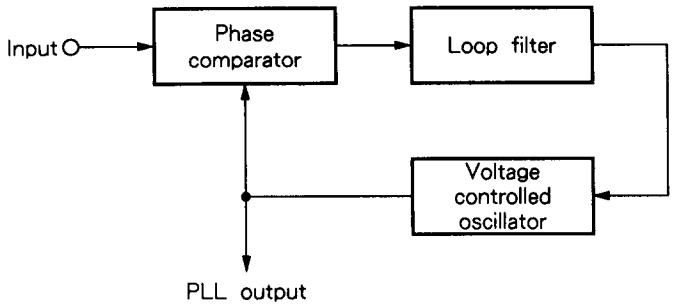


Fig. 5-2. Structure of Analog PLL Circuit

In the past, the analog PLL required circuit adjustments, etc. due to the degradation of phase difference, and other faults caused by aged deterioration of VCO, change in temperature, changes in frequency due to the power supply variation.
The digital PLL (DPLL), a digital PLL, has thus been developed.
The features of the digital PLL (DPLL) are as follows.

- Not affected by voltage amplification changes of input signal.
- Changes in free running frequency due to changes in temperature and voltage amplitude changes can be decreased because no analog VCO is used.
- PLL band width and free running frequency can be set externally (microprocessor, etc.).
- Compact size realized by ICs due to use of digital circuits, and adjustments are easy.

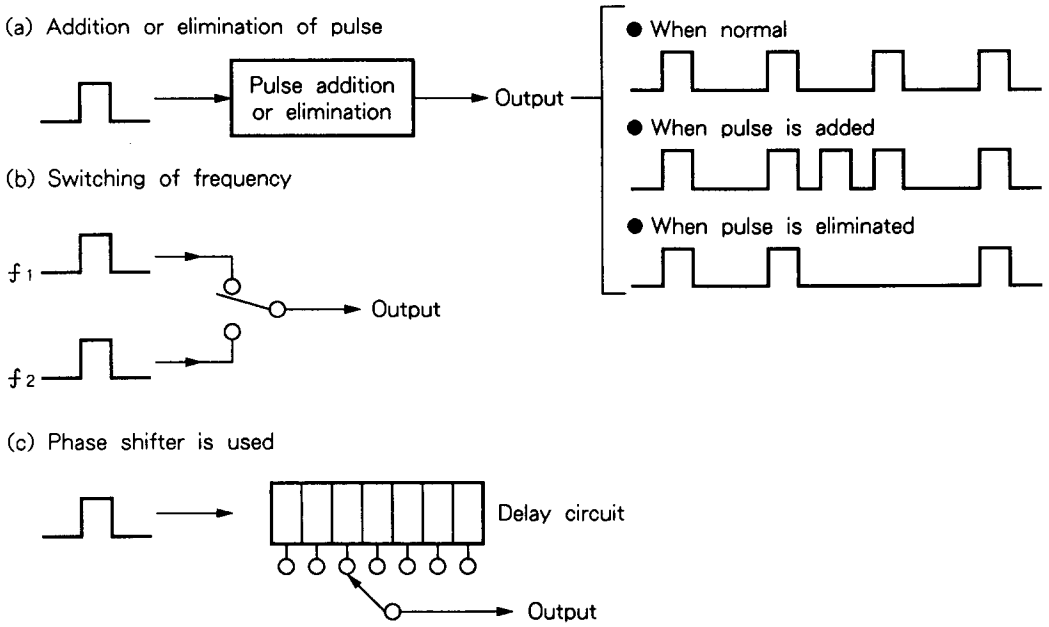


Fig. 5-3. Local Oscillator Circuit of Digital PLL

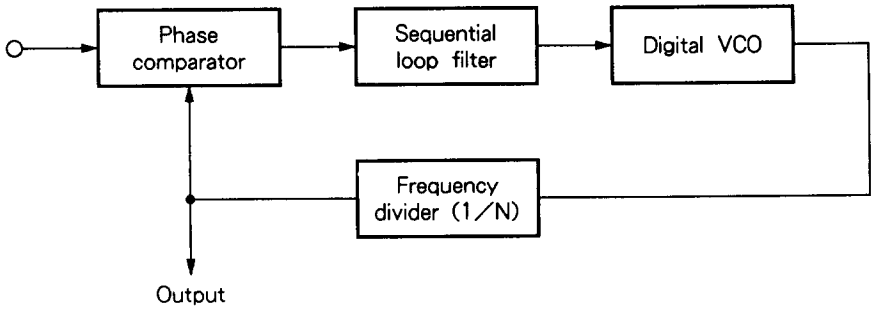


Fig. 5-4. Structure of Digital PLL Circuit

In the digital PLL, the operations of the loop filter and local oscillator are carried out in the digital logic circuit. For example, in the analog PLL, the voltage controlled oscillator is used for the local oscillator, but in the digital PLL, as shown in **Fig. 5-3**, the addition/elimination of the pulse for this output signal is carried out according to (a) the fixed frequency oscillator, (b) several different frequencies are switched, or (c) a phase shifter is provided for the output of the oscillator to switch the output.

The basic structure of the digital PLL circuit is shown in **Fig. 5-4**. Basically, the digital PLL is the same as the analog PLL. The phase comparator outputs digital signals corresponding to the phase difference of the two input signals. The sequential loop filter is similar to the analog PLL loop filter and is composed of the counter. It creates the control signals of the local oscillator from the signal output from the phase comparator.

As the operations of the digital PLL circuit are digital processed according to the clock, the changes in the frequency and phase are not continuous. A frequency divider (I/N) is provided for this output to smoothen the changes. Recently, digital PLLs which perform PLL operations by software processing by A/D converting input signals to digital signals have been developed.

The digital PLL is based on the crystal oscillator, and therefore has the advantage of having high stability. The clock used for the VCO circuit requires frequencies that are several times or above ten times more than the output signal.

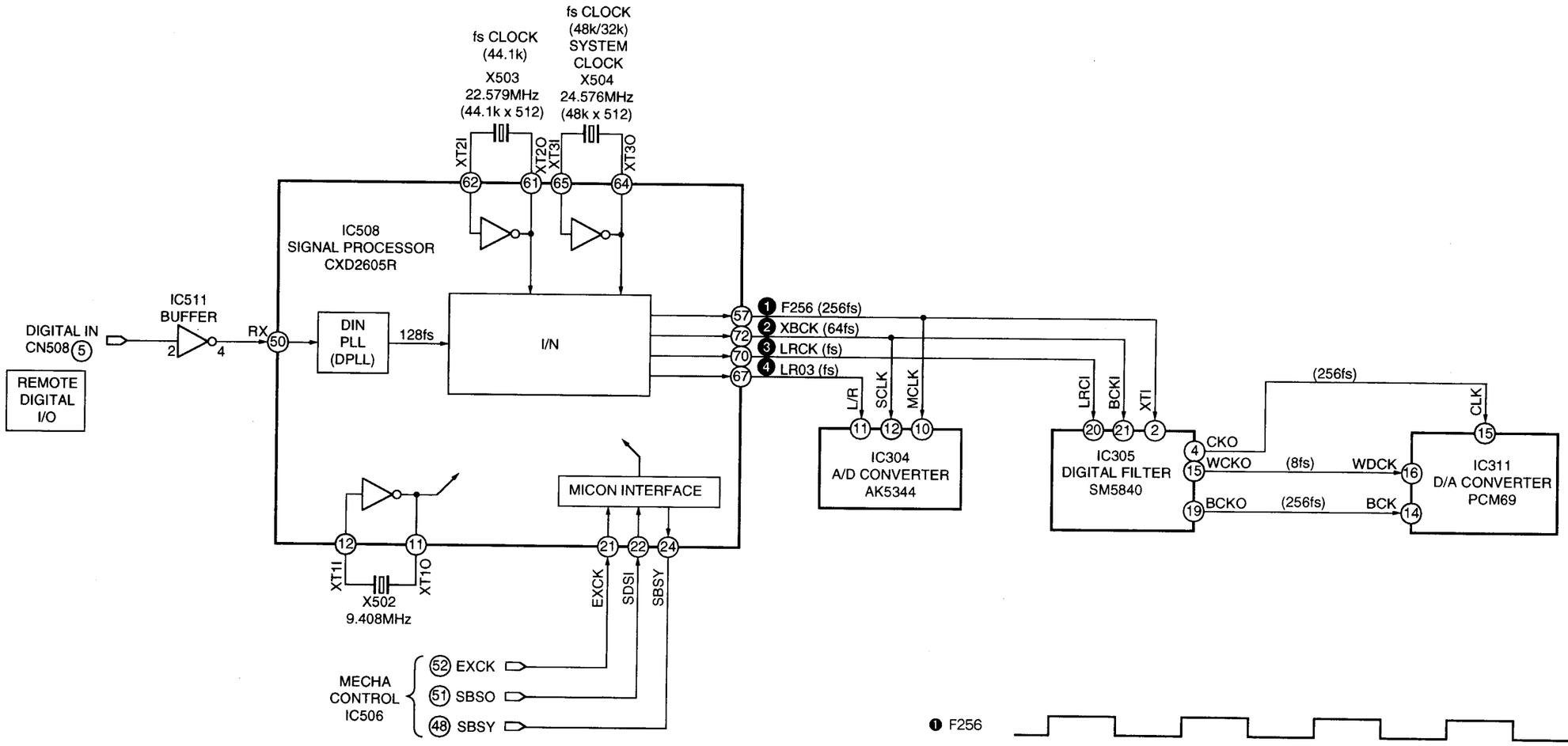
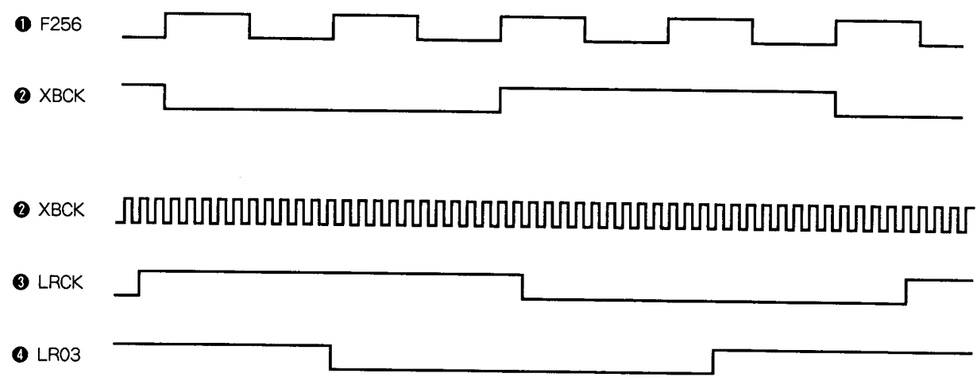


Fig. 5-5 Fs System Clock Block Diagram



Note) During digital recording, F256 is frequency-divided from the X503 or X504 clock. Therefore, the F256 and XBCK are not synchronized.

Clock Timing of Fs System

5-2. Clock System

Fig. 5-5 shows the block diagram of the Fs system clock used in the signal circuit of this system.
The signal processing CXD2605R (IC508) has a recording and playback digital signal processing function, RAM control function, digital I/O signal processing function, and digital IN PLL function. In addition, it also has a function which generates Fs system clocks for obtaining clocks to provide to signal systems such as the BCK (bit clock) and LRCK (L/R clock).
The digital IN PLL has both the analog PLL and digital PLL (DPLL) modes, but this system uses the built-in digital PLL which requires no external parts and consumes little power. **Table 5-1** shows the operations mode of each clock serving as reference. In analog recording and playback, X503 (512 fs, fs = 44.1 kHz) or X504 (512 fs, fs = 48 kHz 768 fs, fs = 32 kHz) is used according to the sampling frequency as the reference frequency. In digital recording, the 128 fs obtained by the digital IN PLL is used as the reference frequency. In the case of digital recording, BCK and LRCK are output by the digital IN PLL by frequency dividing the reference frequency obtained by locking the digital PLL circuit to the sync signal (preamble) in the digital input signal from other equipment such as CD and MD.
At this time, for only F256 (256fs) output from Pin ㊼, as the reference frequency from the digital PLL circuit is 1/2 (128 fs), the X503 or X504 clock is frequency divided according to the sampling frequency and used.
In the operation mode, the reference frequency is switched by the serial data input to Pin ㉒ (SDSI) by synchronizing with the serial clock (EXCK) from the mechanism controller (IC506). X502 (9.408 MHz) connected to Pins ⑪ and ⑫ (XT1I, XT1O) of IC508 are used as the reference oscillation for the 2.352 MHz recording system channel clock in the LP mode, and for the 4.704 MHz recording system channel clock in the SP mode.

Table 5-1. Fs System Reference Clock Operation Mode

Mode	fs (Hz)	X503 (22.5 MHz)	X504 (24.5 MHz)	DPLL (Digital In)
Analog Recording Playback	48k/32k	X	◎	X
	44.1k	◎	○	X
Digital Recording	48k/32k	X	○	◎
	44.1k	○	○	◎

(◎ , ○: Oscillation, X: Oscillation stopped, ◎ : fs reference oscillation)

5-3. Operations During Recording

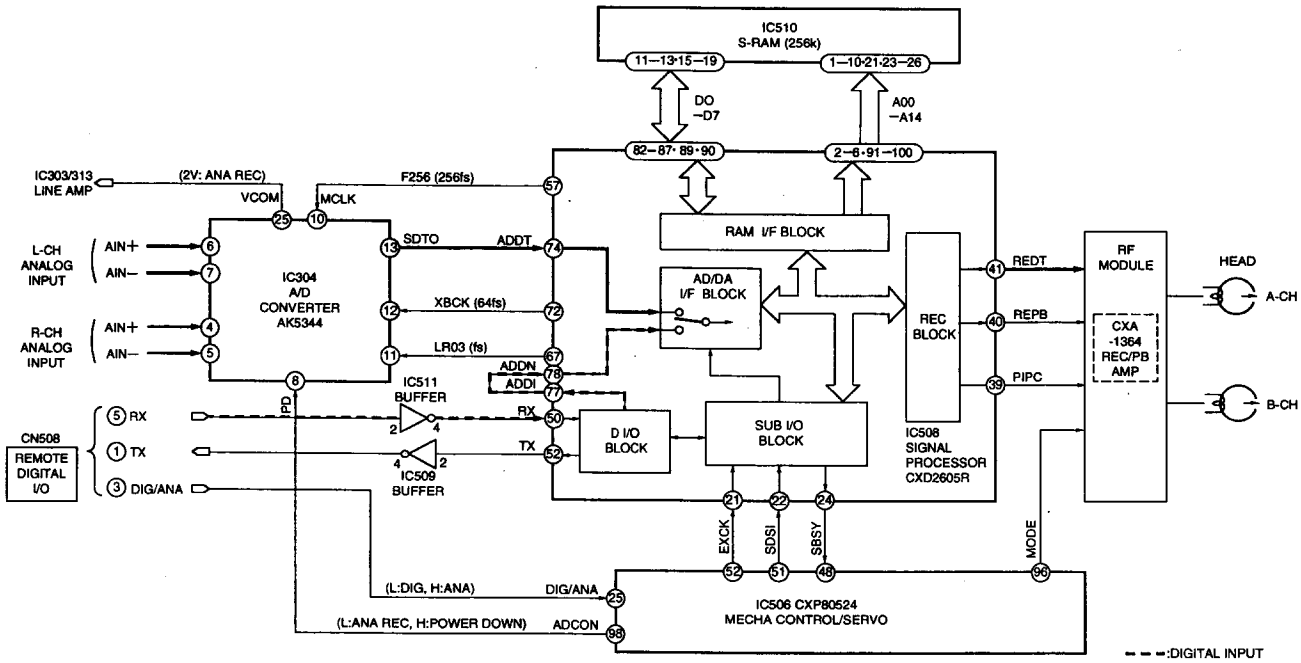


Fig. 5-6. Flow of Recording Signals

The Lch and Rch analog signals input to Pins ⑥ and ⑦ (AINL+, AINL–) and Pins ④ and ⑤ (AINR+, AINR–) of the A/D converter (IC304) are converted to 16 bit digital signals each inside the A/D converter, synchronized with the bit clock (XBCK) and L/R clock (LR03) and output to the signal processor (IC508) from Pin 13 (SDTO) for Lch and Rch alternately. For the A/D converter, a x64 oversampling compatible ΔΣ(1 bit) format AK5344 operating on a single power supply (+4V) is used. As the analog input signal is input to the non-inverted (AIN+) and inverted (AIN–) differential circuit, the input circuit is, as shown in **Fig. 5-7**, connected through a buffer to the single end/differential inverted circuit composed of the inverted circuit.

Therefore, this input voltage is the AIN+ and AIN– differential voltage {ΔVAIN = (AIN+)–(AIN–)}. During analog recording, a 2V bias voltage equivalent to 1/2 of the power supply voltage is supplied to the non-inverted input pins of the differential inverted circuit from Pin ㉕ (VCOM) of the A/D converter. The A/D converter only operates during analog recording, and controls power consumption at other times by setting into the power down mode. This control is performed by Pin ㊽ (ADCON) of the mechanism controller.

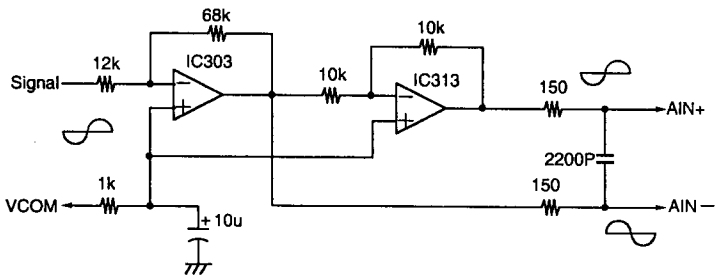


Fig. 5-7. Differential Conversion Circuit

In the signal processor (IC508), the MAIN-ID, SUB-ID, and sub data (PACK data), etc. from the mechanism controller (IC506) are synchronized with the clock (EXCK) and input to Pin ㉒ as the serial data (SDSI).
Each signal is interleaved by the signal processor (IC508) and S-RAM (IC510), added with the C1 parity and C2 parity, 8-10 modulated in the REC block, added with the ATF signal, and output from Pin ㊶ (REDT) to the RF module. In the RF module, the recorded data (REDT) is amplified in the recording amplifier, and transmitted to head A and head B alternately as the recording signal at the timing of the switching pulse (SWP) as shown in **Fig. 5-8**.
The head recording/playback amplifier inside the RF module is switched between recording and playback according to the MODE signal from Pin ㊽ of the mechanism controller and recording/playback identification signal (REPB) output from Pin ㊵ of the signal processor. When these signals are "H", the amplifier is set to the recording mode, and when "L", it is set to the playback mode. (For details, refer to 5-5. RF Module.)
The PIPC signal output from Pin ㊴ of the signal processor indicates the recording area of the ATF pilot signal. Inside the RF module, the recording level of the ATF pilot signal is set by this signal.

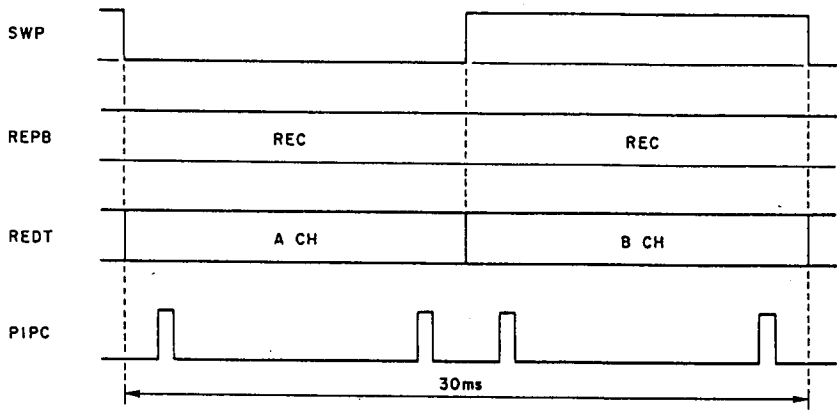


Fig. 5-8. Timing of Signals during Recording (SP Mode)

Digital Recording
In digital recording, the digital audio interface format signal transmitted from the other equipment is input to Pin ㊿ (RX) of the signal processor (IC508) via the buffer (IC511) from Pin ⑤ of the digital I/O connector (CN508).
Data is fetched by the clock generated in digital IN PLL circuit of the DI/O block and the audio data is transmitted to the AD/DA I/F block. Control information supplied such as emphasis ON/OFF, copy permit/prohibit, etc. is transmitted to the mechanism controller via the SUB I/O block. The switching of the analog input and digital input from the A/D converter is performed as follows. When the analog/digital switch at the accessory (POC-DA12 and RM-D3K, etc.) connected to the digital I/O connector (CN508) is set to the digital side, Pin ㉕ (DIG/ANA) of the mechanism controller becomes "L", and this will cause the serial data (SDSI) of the digital IN REC from Pin ㊶ to be output to the signal processor (IC508) and switch the inputs.

5-4. Operations during Playback

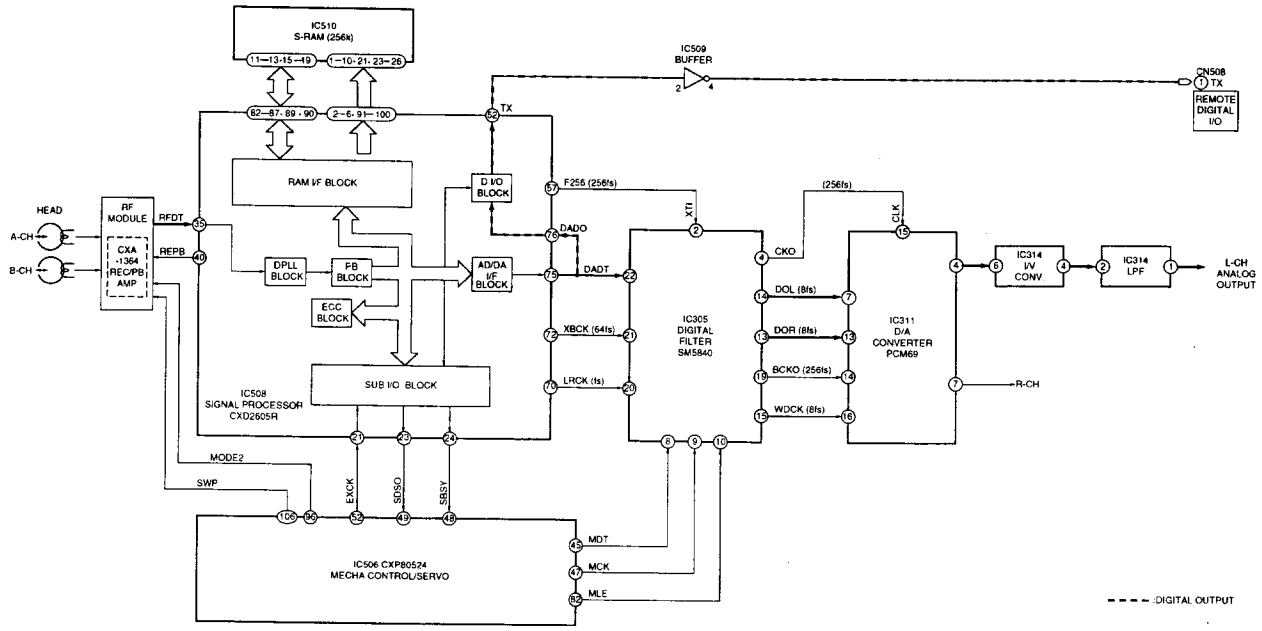


Fig. 5-9. Flow of Playback Signal

Fig. 5-9 shows the flow of the playback signal, and **Fig. 5-10** shows the signal timing during playback.
The playback RF signal (RFDT) from heads A and B are input to the RF module according to the timing of the switching pulse (SWP) as shown in **Fig. 5-10**, and then amplified by the playback amplifier inside. The RF signal is then synchronized with the clock generated from the RF data (RFDT) by the digital PLL (DPLL) inside the signal processor (IC508), input to the PB block, where 10-8 demodulation opposite to that in recording is performed. Deinterleaving is then performed by the signal processor (IC508) and S-RAM (IC510), followed by error detection and error correction in the ECC block. The audio data is transmitted to the digital filter (IC305) from Pin ⑮ (DADT) and the sub code data is transmitted from Pin ㉓ (SDS0) to the mechanism controller (IC506) via the SUB I/O block.
The digital filter performs x8 oversampling for 16 bit audio data to convert the data to 18 bits and then performs filter operation. The Lch synchronizes with the bit clock (BCK) and word clock (WDCK) from Pin ⑭ (DOL) while the Rch synchronizes with the same clocks from Pin ⑬ (DOR), and are output to the D/A converter in parallel format.
In addition to these functions, the digital filter has a digital emphasis function, digital attenuate function, etc. These are set together with internal initial settings by the mode setting data (⑧MDT) input by synchronizing with the mode set clock (⑨ MCK) and mode latch enable (⑩MLE) signals.

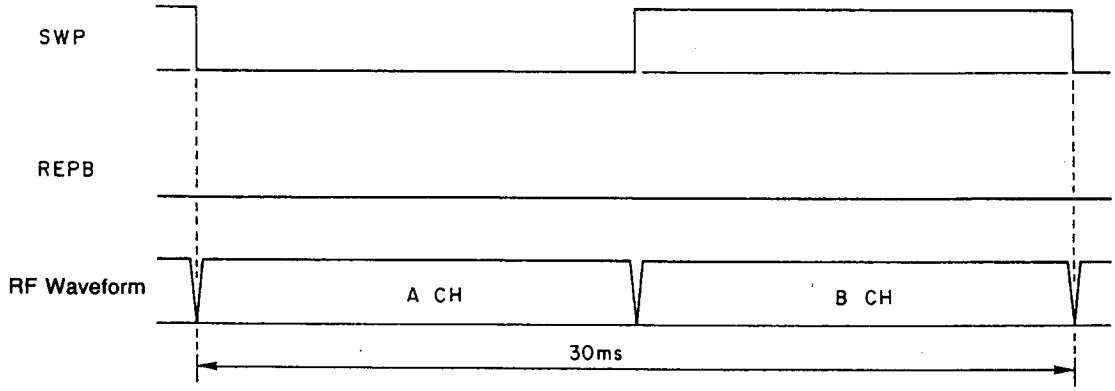


Fig. 5-10. Signal Timings (SP Mode) During Playback

Digital Output

The digital data is the audio data input from Pin ⑮ to Pin ⑯ and the serial data (SDSO) from the mechanism controller, etc. and information such as category codes input to the SUB I/O block are bit arranged into the digital audio interface format by the D I/O block. After the 28 bits excluding the sync pattern (preamble) is* biphase mark-modulated, it is output from Pin 1 of the digital I/O connector (CN508) via the buffer (IC509) from Pin ⑫ (TX).

* With this modulation method, as shown in **Fig. 5-11**, when the data bit is "1", the phase is inverted at the center of the bit. It is not inverted when the data bit is "0".

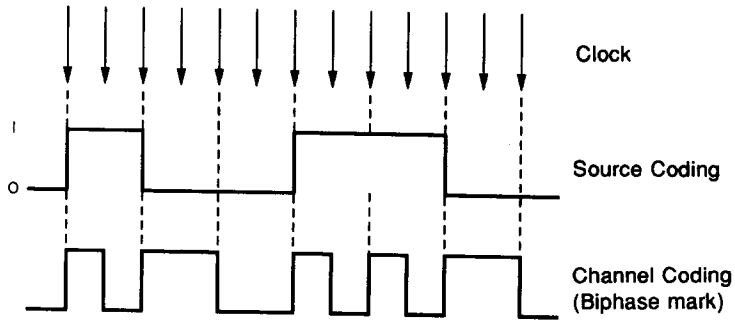


Fig. 5-11. Biphase mark Modulation

5-5. RF Module

Fig. 5-12 shows the internal circuit of the RF module.

As shown in the figure, the RF modules incorporates a recording/playback amplifier CXA1364. The operation mode is switches as shown in **Table 5-2** by the MODE 2 (operation mode switching signal) from the mechanism controller (IC506) and the REPB (recording/playback switching signal) from the signal processor (IC508). The SWP (switching pulse) is used for the switch amplifier which switches the output from the A/B head amplifier at the SWP timing during playback.

The controls inside are adjusted to the optimum values of the head drums used as a pair for adjusting the PCM and pilot recording current of channels A and B. (This adjustment and the internal repair of the RF module are not performed as servicing.)

Table 5-2. RF Module Operation Mode

Mode	CN501		
	⑨ MODE 2	⑥ REPB	⑧ SWP
Recording	H	H	"L" : Head A is in recording mode "H" : Head B is in recording mode
Playback	L	L	"L" : Head A is in playback mode "H" : Head B is in playback mode

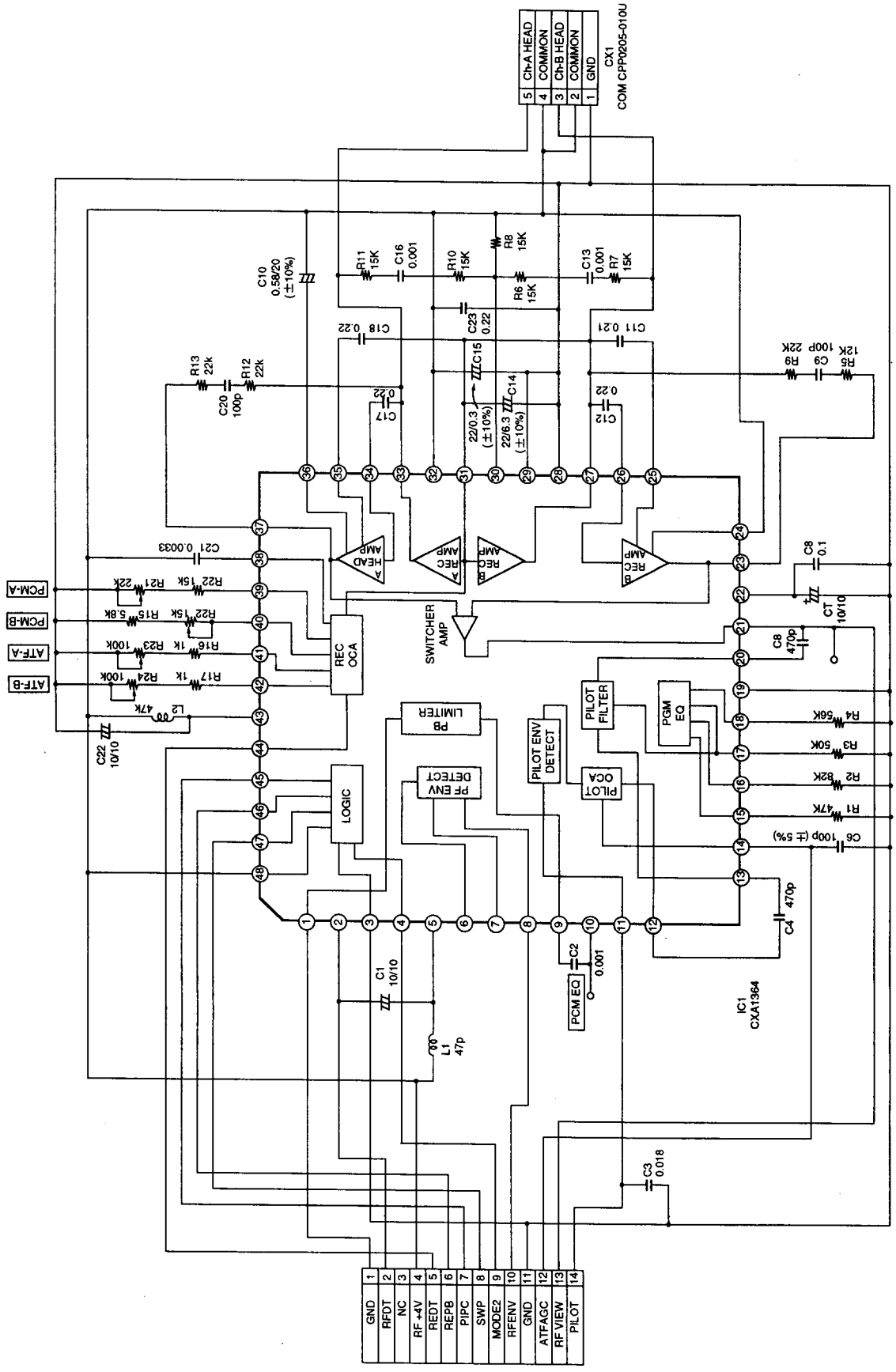


Fig. 5-12. RF Module Internal Circuit

6. SERVO CIRCUIT

6-1. Outline of Servo Circuit

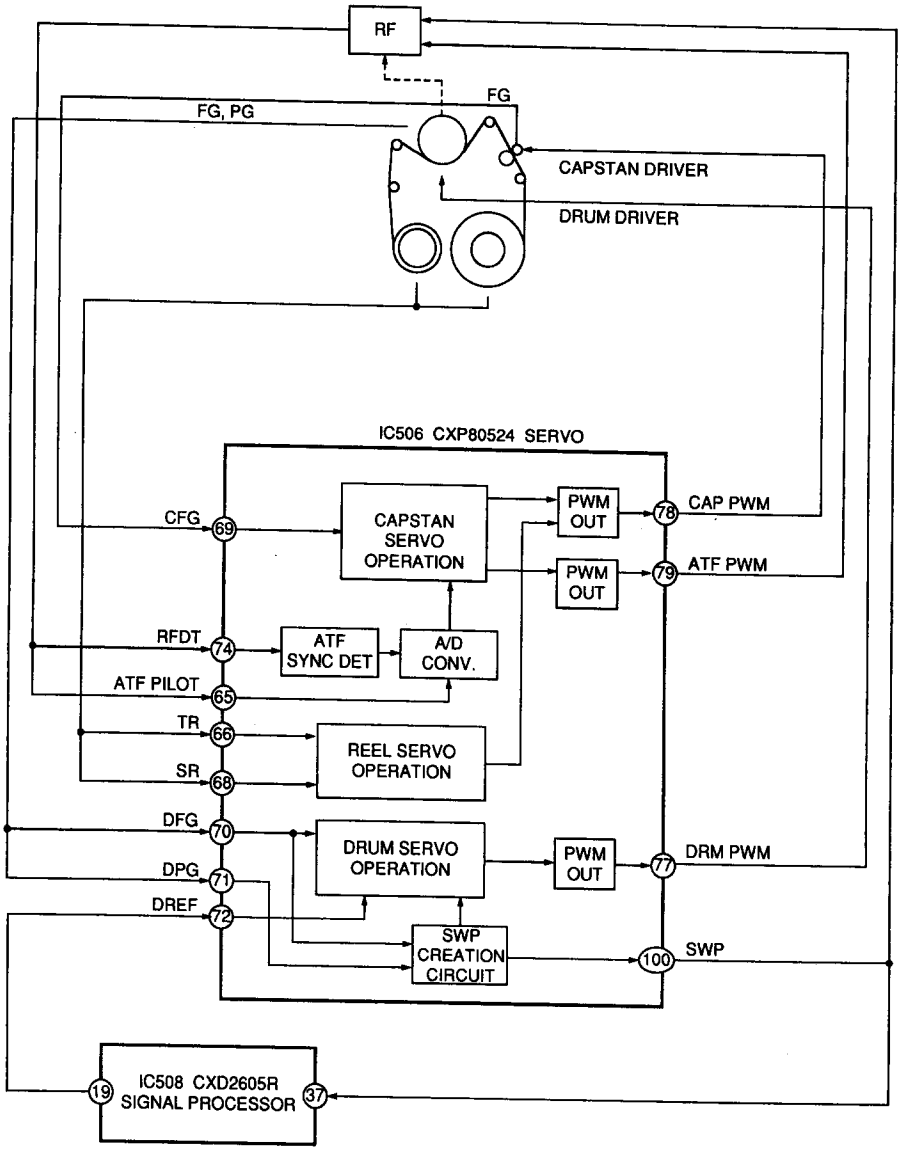


Fig. 6-1. Outline of Servo Circuit

The servo block, as shown in **Fig. 6-1**, is composed of the capstan servo which controls the tape running speed to a constant speed using the capstan FG (CFG), ATF servo which controls so that the head runs the designated track properly with the ATF signal from the playback track, the reel servo which controls high speed tape running such as FF/REW, search, etc. to a constant speed using the reel FG (TR, SR) signals, and the drum servo which controls the drum rotation to a constant speed using the FG and PG (DFG and DPG) signals from the drum. A software servo is employed for these servo using the servo microprocessor (CXP80524) inside the special hardware.
The ATF PWM signal in the diagram is used to prevent incorrect operations of the ATF servo caused by differences in the recording currents of the tape played back by performing automatic adjustment (ATF AGC) of the RF amplifier gain.

This system uses a head drum with a diameter of 15 mm.
Table 6-1 shows the drum rotation, tape speed, etc. of each mode.
As shown in this table, the drum rotation in the LP mode is 1000 rpm in the recording mode and 2000 rpm (two times) in the playback mode. Consequently, the same head playback output as the SP mode can be obtained. As the transmission rate during playback in the LP mode is same as the SP mode, there is no need to change the constant for playback EQ (equalizer) and PLL circuit, etc. for each mode. Although the head will not be on-track precisely during playback, because the same track is read twice, the data which has been read better will be taken as the effective data. During playback in the LP mode, as the trace angle of the head is slightly smaller than the track pattern on the tape, if the sub code is after-recorded in this state, the data can not be written in the original sub code area correctly.
Therefore, during after-recording of the sub codes in the LP mode, the tape speed is set to 8.15 mm/s as in the SP mode so that the data is recorded with the track pattern and trace angle of the head matched.

Table 6-1. Specifications in Use of 15 mm Diameter Drum

Mode		Drum Rotation (rpm)	DREF (Hz)	Tape Speed (mm/s)	Transmission Rate (Mbps)
SP	Recording	2000	100/3	8.150	4.704
	Playback	2000	100/3	8.150	4.704
	Sub Code After-Recording	2000	100/3	8.150	4.704
LP	Recording	1000	50/3	4.075	2.352
	Playback	2000	50/3	4.075	4.704
	Sub Code After-Recording	2000	100/3	8.150	4.704

SP: Standard Play Mode
LP: Long Play Mode
DREF: Drum Reference

6-2. Capstan (Reel) Servo Circuit

The capstan motor is used for running the tape at constant speed between it and the pinch roller, loading and unloading the tape and mechanism section, and driving the T and S reel tables. The servo using the capstan motor is, as shown in **Table 6-2**, broadly divided into the capstan servo and reel servo.
The relation of the modes for each capstan speed is as shown in the table. For x0.5 to x8, the capstan servo by CFG is used mainly for controlling the speed during tape running. In the high speed running of x25 used in high speed CUE/REV, and of x25 to x100 used for FF/REW and search, the rotation of the capstan motor is controlled by the FG (TR, SR) signals from the T and R reel tables so that the tape running speed becomes constant.
The x8 measure mode is used for measuring the total length of the tape in FF/REW and search immediately after the cassette is loaded. Based on this, the remaining tape and reel servo speed is calculated. (In the normal playback state, these are measured by the speed corresponding to the LP or SP mode.)

Table 6-2. Capstan Speed and Main Purposes

Servo Type	Speed	CFG (Hz)	Main Purpose
Capstan Servo (Servo by CFG)	x0.5	296	LP mode
	x1	592	SP mode
	x1.5	888	Software tape
	x3	1.776	CUE/REV, LOAD UNLOAD
	x8	4.736	Measure mode
Reel Servo (Pinch roller does not press due to reel FG servo)	x25		High speed CUE/REV
	x25 to x100		FF/REW search

Circuit Operations

As shown in the block diagram in **Fig. 6-2**, the FG signal from the capstan motor is waveform-shaped in the sensor amplifier (IC504) and then input to Pin ⑰ (CFG) of the CXP80524 (IC506). In the CXP80524, comparison and servo calculation are performed by the reference clocks generated by this capstan FG (CFG) and MCLK (master clock) to detect the speed error. This is output from Pin ⑱ (CAPPWM) as the reference waveform 36.7 kHz PWM output. During playback, only the ATF pilot signal (130 kHz) from the playback waveform (RF) of the RF module is filtered. Using the ATF sync signal obtained from the envelope (ATF PILOT) signal input to Pin ⑮ (ATFPLT) and RFDT signal input to Pin ⑭ (RFDT), the tracking error is detected and output as the PWM waveform together with the speed error.
During playback in the LP mode, because the drum speed is increased to two times (2000 rpm) that in recording, the heads trace the tracks twice at a transit angle different from the REC angle.
Control using the software is carried out so that only the just track part is imposed with the ATF servo.
For the reel servo used in FF/REW and search, the FG signal from the reel sensor attached below the T and S reel tables is waveform-shaped by the sensor amplifier like the capstan FG and input to the CXP80524 reel calculation circuit.
In this calculation circuit, the period and period ratio are detected using the two reel FG (TR and SR) signals, and the optimum speed at this position is calculated according to the tape length and tape position data obtained in the measure mode, and output in the PWM waveform.
The PWM waveform is passed through the LPF and PWM drive (IC501), buffer (Q502), and motor drive (IC503) to drive the capstan motor.
Pin ④ of IC 506 (CAPDIR) is an output pin which controls the direction in which the capstan motor rotates. When "H", it rotates the capstan motor in the FWD direction. Q3001 connected to Pin ⑯ (ANGL) of the drive (IC503) mutes the output from U to W OUT so that the capstan motor does not operate unnecessarily when the Vs input of Pin ㉙ is 0V. The ATF AGC signal output from Pin ⑲ (ATFPWM) detects the level of the ATF PILOT signal input to Pin ⑮, and gain-adjusts the PILOT GCA (gain control amplifier) inside the RF module to correct the level of the pilot signal due to the difference in the recording current of the tape played back.

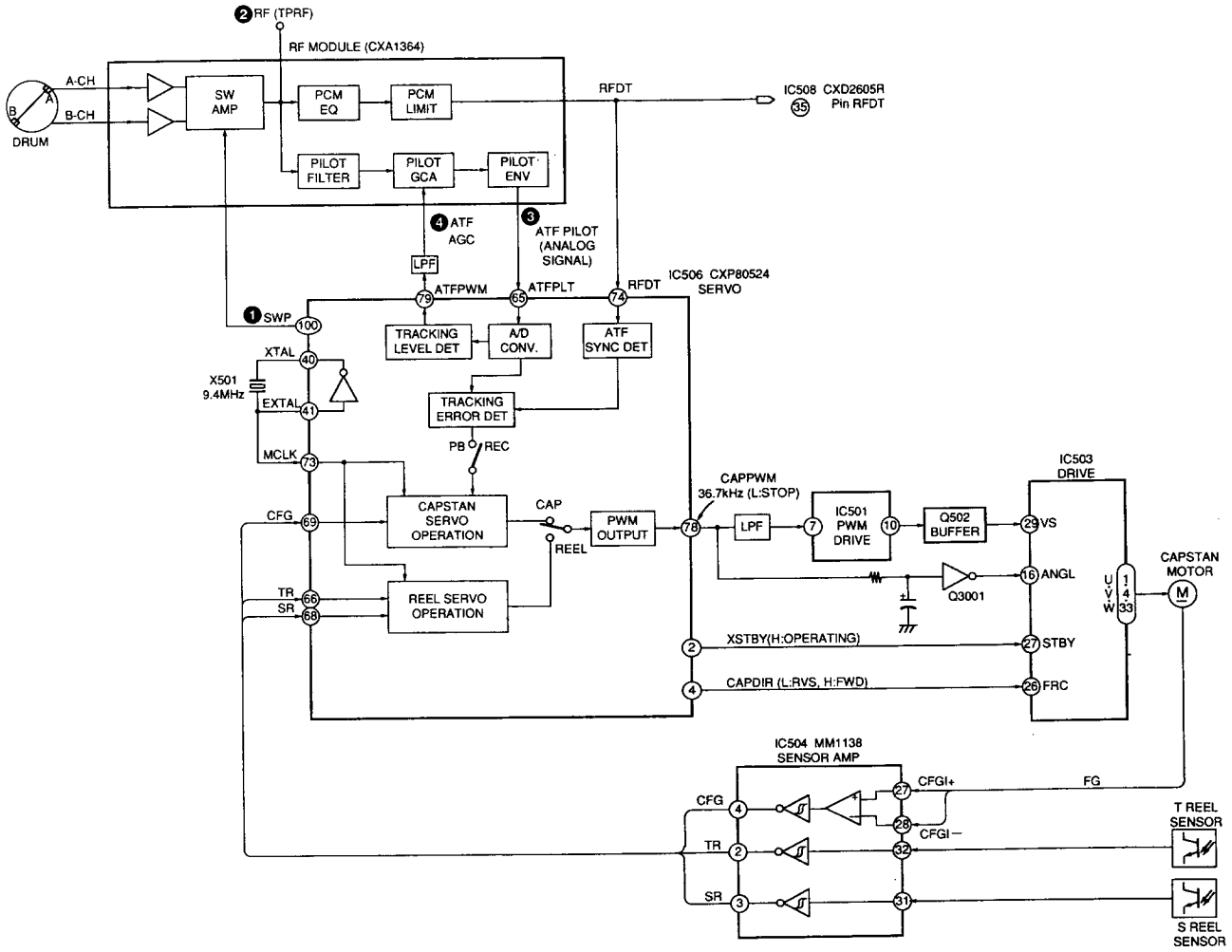


Fig. 6-2. Block Diagram of Capstan Servo

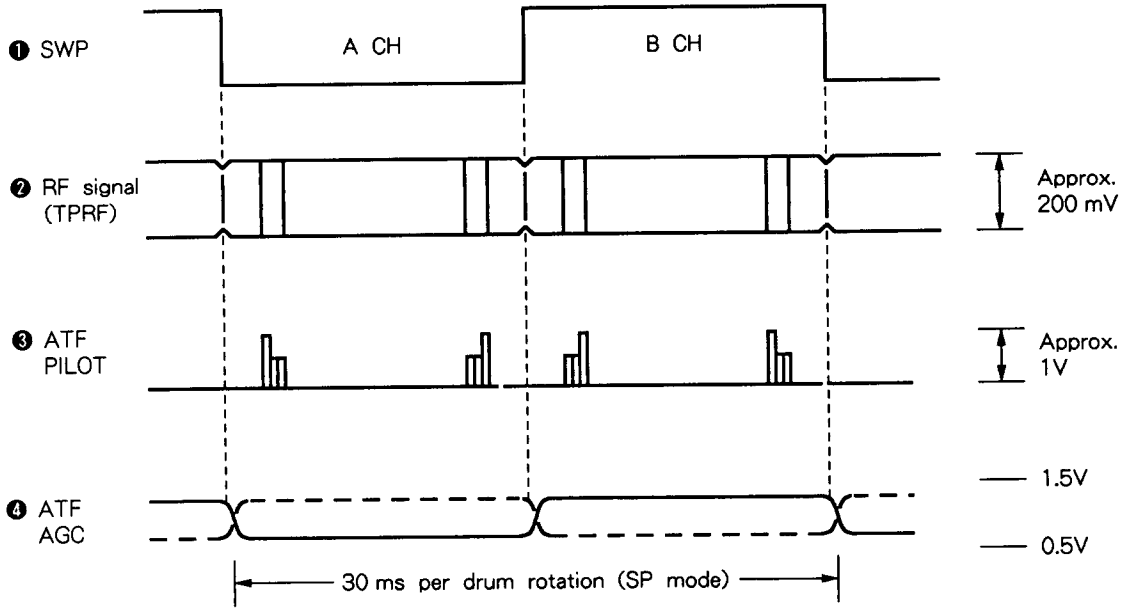


Fig. 6-3. Capstan Servo Waveform Timing (Reference Value)

6-3. Drum Servo Circuit

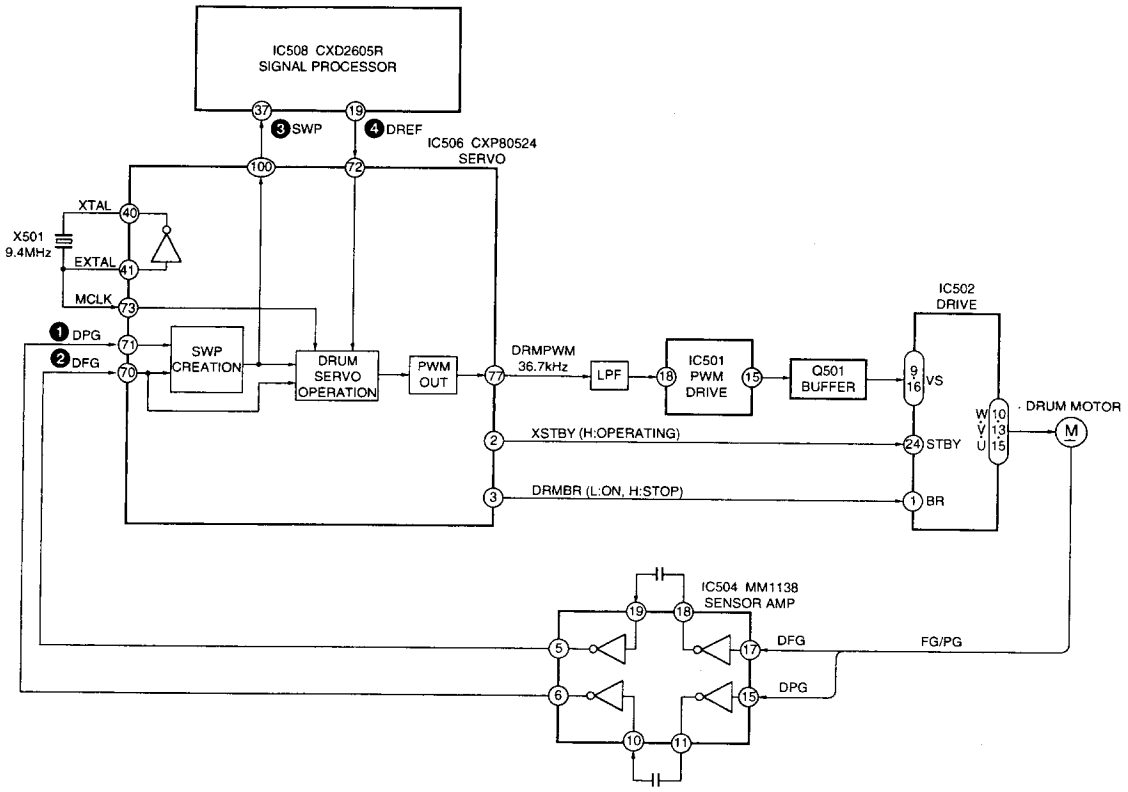
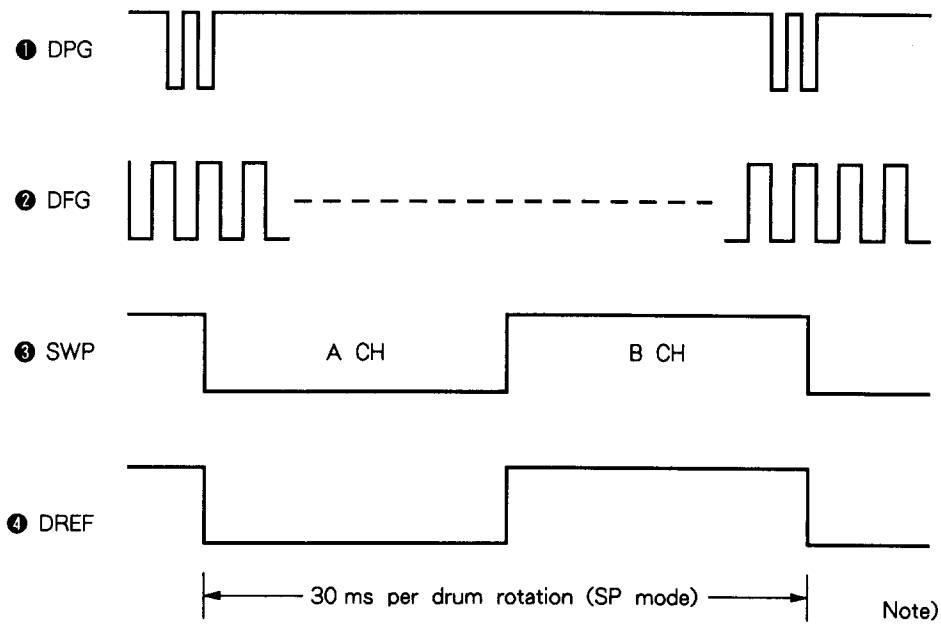


Fig. 6-4. Drum Servo Block Diagram



Note) The phase difference between DPG and SWP (DREF) changes according to the adjustment of RV501 (SWP).

Fig. 6-5. Drum Servo Waveform Timing

Operations of Circuit

The FG and PG signals from the drum motor are first waveform-shaped by the sensor amplifier (IC504), after which FG is input to Pin ⑦⓪ (DRMFG) of CXP80524 (IC506) and PG is input to Pin ⑦① (DRMPG). Inside the CXP80524, the SWP (switching pulse) is generated from these two signals. The reference signal DREF (drum reference) of the drum servo made inside the signal processor CXD2605R is input to Pin ⑦② (DREF). In the drum servo calculation block, the period of the DFG signal is calculated to detect the speed error, or the phase of SWP and DREF is compared to detect the phase error. This error signal is converted to a reference waveform 36.7 kHz PWM waveform in the PWM output in the next stage, output from Pin ⑦⑦ (DRMPWM), converted to an analog signal in the PWM driver (IC501), and input to the drum motor drive (IC502) via the buffer (Q501) to control the rotation of the drum motor.

Table 6-3. Main Frequencies of Drum Servo (During Servo Lock)

Mode		DREF (Hz)	SWP (Hz)	DFG (Hz)
S P	Recording	100/3	100/3	800
	Playback	100/3	100/3	800
L P	Recording	50/3	50/3	400
	Playback	50/3	100/3	800

SP : Standard Play Mode
LP : Long Play Mode
DREF : Drum Reference
SWP : Switching Pulse
DFG : Drum Frequency Generator

When the drum servo is in the lock state, the drum rotation number is, as shown in **Table 6-1**, 2000 rpm for both recording and playback in the SP mode. In the LP mode, it is 1000 rpm during recording and 2000 rpm during playback. In these speeds, the frequency of DREF, SWP, and DFG are as shown in **Table 6-3**. The signal timing in the SP mode is as shown in **Fig. 6-6**. In both recording and playback, the DREF and SWP have the same phase. The recording data (REDT) during recording and discrimination signal (PIPC) which indicates the pilot area of ATF are output from the signal processor CXD2605R (IC508), and the RF signal during playback is output from the RF module, both at the timing at which they synchronize with the DREF and SWP.

As for the timing of the LP mode signals, as shown in **Fig. 6-7**, because the drum rotation number during recording is half that in the SP mode, the period of these signals is twice those in the SP mode. During playback, because the drum rotation number is set to the same in the SP mode (2000 rpm), the period of the SWP and RF signals is made the same as that in the SP mode. The envelope of the RF signal during playback is not flat because the trace angle differs due to the difference in the drum rotation numbers of recording and playback. A and A' and B and B' indicate the RF signals of the same tracks.

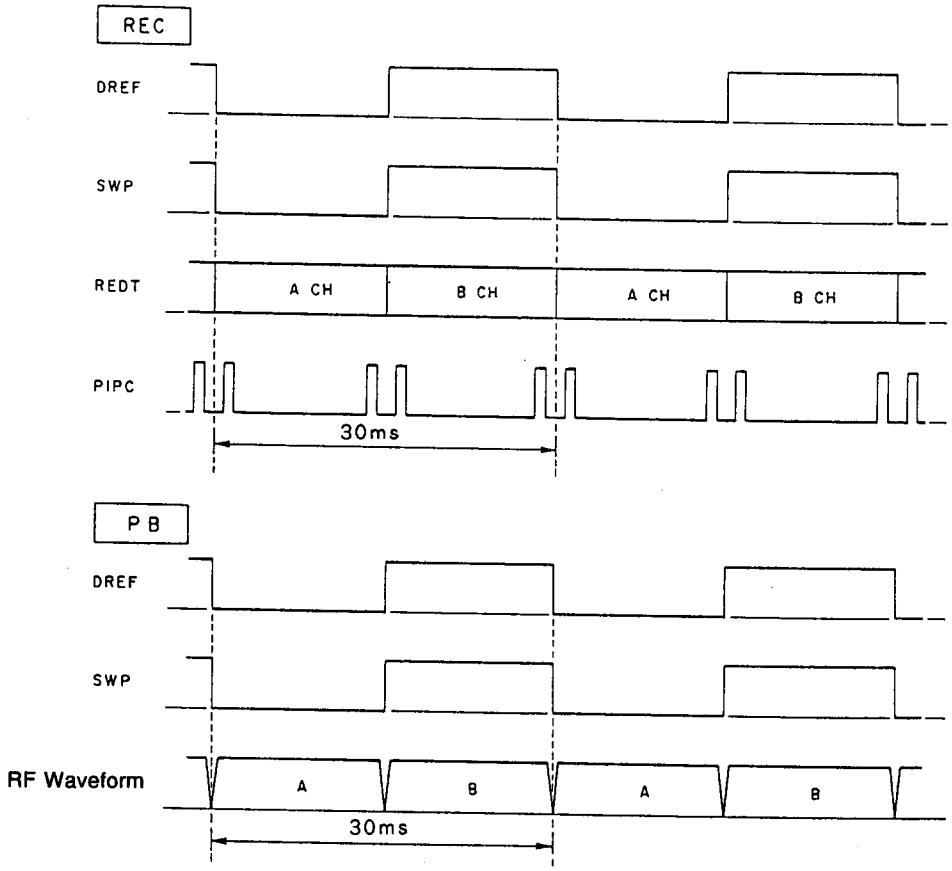


Fig. 6-6. Signal Timing (SP Mode)

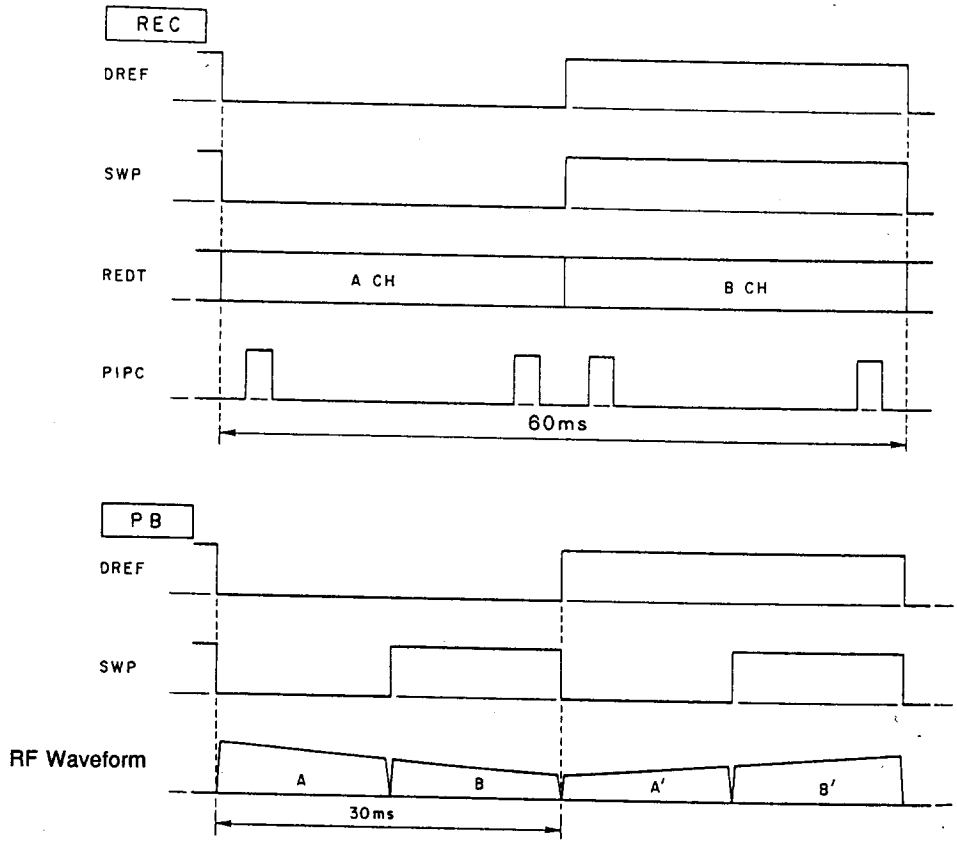


Fig. 6-7. Signal Timing (LP Mode)

7. MECHANICAL CONTROL CIRCUIT

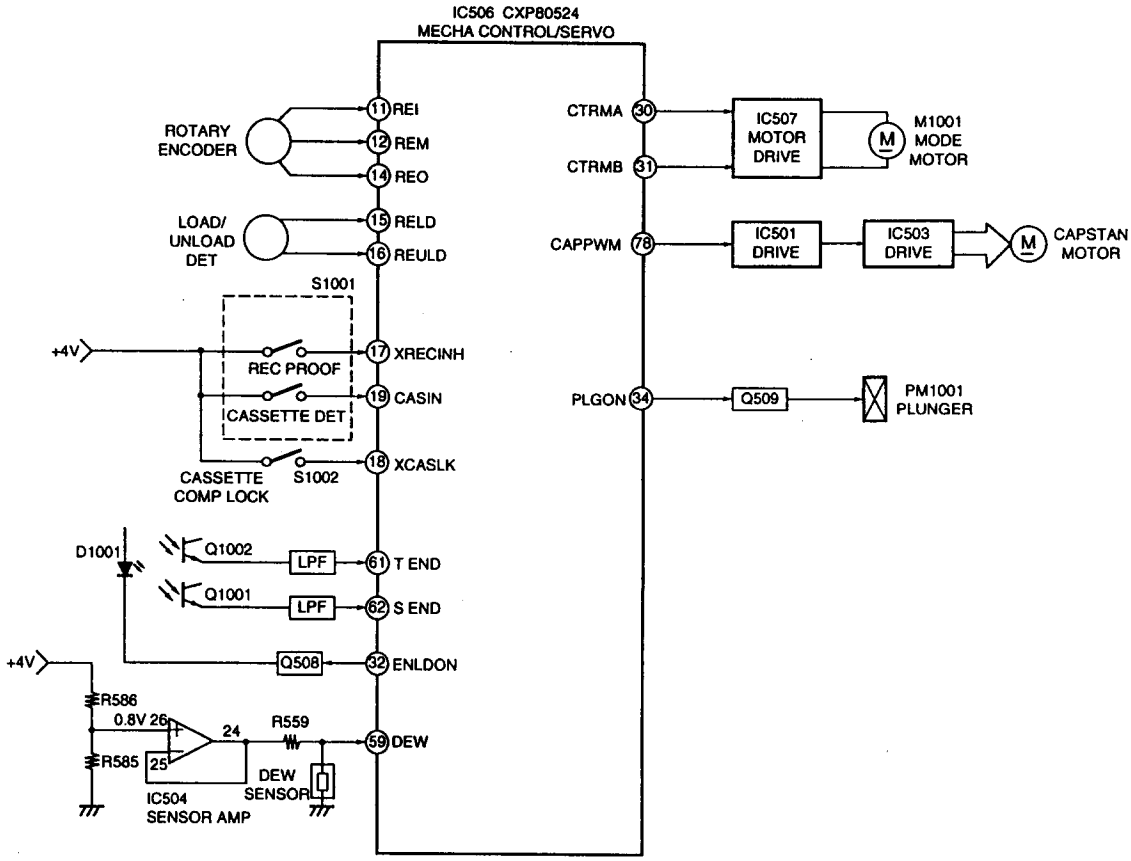


Fig. 7-1. Outline of Mechanical Control

This system uses the CXP80524 (IC506, mechanism controller/servo) as its main microprocessor. Its control can broadly be divided into the following three items.

- Mechanical control (control of mechanism deck and generation of internal mode)
- Serial data control (communication control such as sub code data, display microprocessor I/O, etc.)
- Servo control (drum, capstan software servo)

As shown in the outline provided in **Fig. 7-1**, all the mechanical control is performed by the CXP80524. The mechanism mode is set by the driving of the mode motor, and detected by the rotary encoder. Loading and unloading operations are performed by driving the gear (loading) with the capstan motor, and detected by the same gear (LOAD/UNLOAD DET). The END LED (D1001) and END sensors (Q1001, 1002) detect the top/end of the tape. The LEDs are driven by pulse lighting only about 10 minutes before the tape top and end to save power.
Detection of condensation is carried out by the DEW sensor which is attached to the mechanism block with the voltage corresponding to the changes in the resistance of the DEW sensor (resistance increases with humidity) based on the voltage (0.8V) obtained by dividing resistance.
In FF and REW, the MECHANICAL mode (release of brake of both reel tables) is maintained using a plunger (PM1001) due to the characteristics of the mechanism deck.

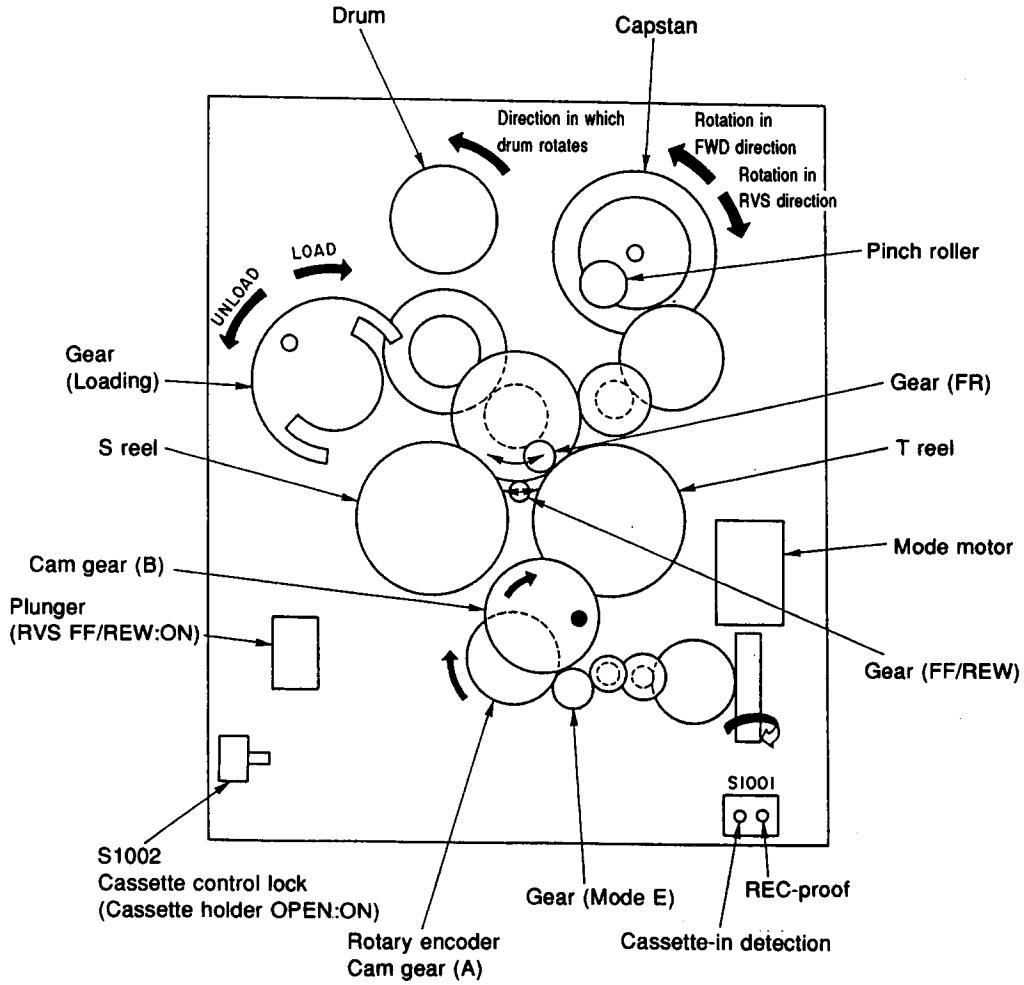


Fig. 7-2. Main Parts of Mechanism Deck (Front View)

Fig. 7-2 shows the position of the main mechanism parts as seen from the front of the mechanism deck. The mechanism deck of this system has three motors and three switches. Their main uses are as follows.

Motor	Main Uses
Drum motor	Head drum driving
Capstan motor	Tape conveyance (FWD/RVS direction), T and S reel tables driving, Tape running system loading/unloading
Mode motor	Setting of mechanism mode

Switch	Uses (Connected to what and truth value when ON)
S1001 (Right)	Rec-proof hole detection (ON: Rec-proof hole closed, recording possible ..... →IC506⑰"H")
S1001 (Left)	Cassette-in detection (ON: Cassette is present ..... →IC506⑲"H")
S1002	Cassette control lock detection (ON: Cassette holder OPEN ..... →IC506⑱"H")

7-1. Mode Motor Control

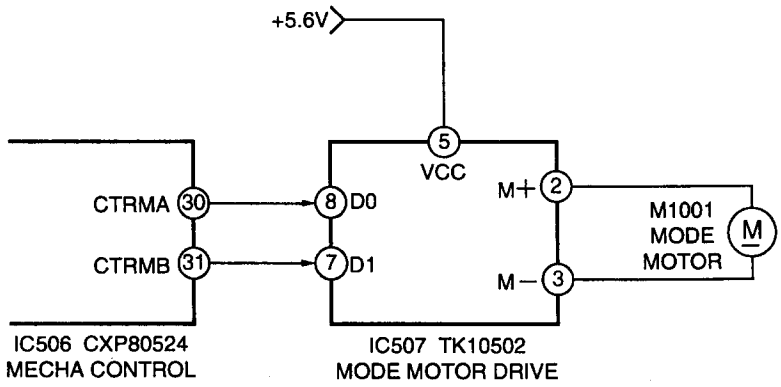


Fig. 7-3. Mode Motor Control Circuit

The mode motor (M1001) which sets the mechanism modes is controlled by Pin ㉚ (CTRMA) and Pin ㉛ (CTRMB) of the mechanism controller/servo (IC506) via the motor drive TK10502 (IC507). The mode motor drive operations are, as shown in **Table 7-1** (TK10502 truth table), free when both input pins ⑧ and ⑦ are "L", and set to the modes shown when the mode motor is in the stop state. When Pin ⑧ (D0) is "H", the mode motor rotates in the normal direction, and the cam gear (B) of the front side of the mechanism deck rotates in the clock direction. When Pin ⑦ (D1) is "H", the mode motor rotates in the opposite direction and the cam gear (B) rotates in the counterclockwise direction. Furthermore, when both input pins ⑧ and ⑦ are "H", the mode motor is set to the brake mode to stop the motor promptly after the end of the mode-shift operations of the mechanism.

Table 7-1. Mode Motor Drive TK10502 Truth Table

Input		Output		Mode Motor Operations
⑧ D0	⑦ D1	② M+	③ M−	(Arrow shows direction of flow of current)
L	L	L	L	Free
H	L	H	L	② M+ → ③ M− (Normal direction)
L	H	L	H	② M+ ← ③ M− (Reverse direction)
H	H	L	L	Brake

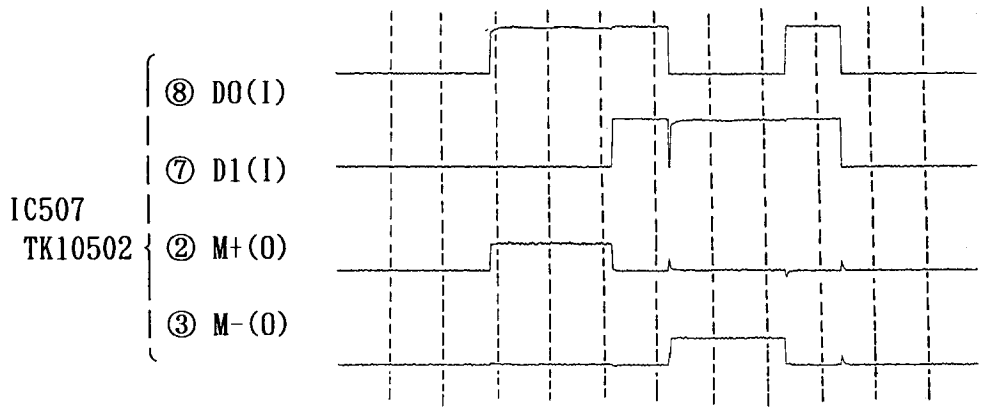


Fig. 7-4. Motor Drive Input/Output Waveform (Example of OPEN, 100 ms/div)

7-2. Load/Unload Completion Detection

Loading and unloading are performed by rotating the gear (loading) shown in **Fig. 7-2** in the normal and reverse direction. Using the capstan motor via the four gears, loading is performed by rotating the capstan motor in the FWD direction and unloading by rotating it in the RVS direction. The completion of loading and unloading is detected by a sliding element with two contacts attached at the back of the gear (loading). The sliding element detects completion by sliding on the electrode patterns shown in **Fig. 7-5** and connecting the COM pattern to which +4V power is added and REULD or RELD pattern. If the loading or unloading does not complete 4 seconds after the capstan motor has been started up, it is determined as error, and error code "10" is displayed on the LCD if loading did not complete, and error code "11" is displayed if unloading did not complete.

Fig. 7-6 shows input waveform timings of the mechanism controller (IC506) pins during loading and unloading operations.

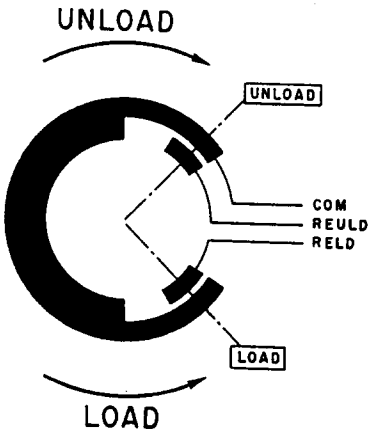


Fig. 7-5. Electrode Patterns of Gear (Loading)
(Rear View of Mechanism Deck)

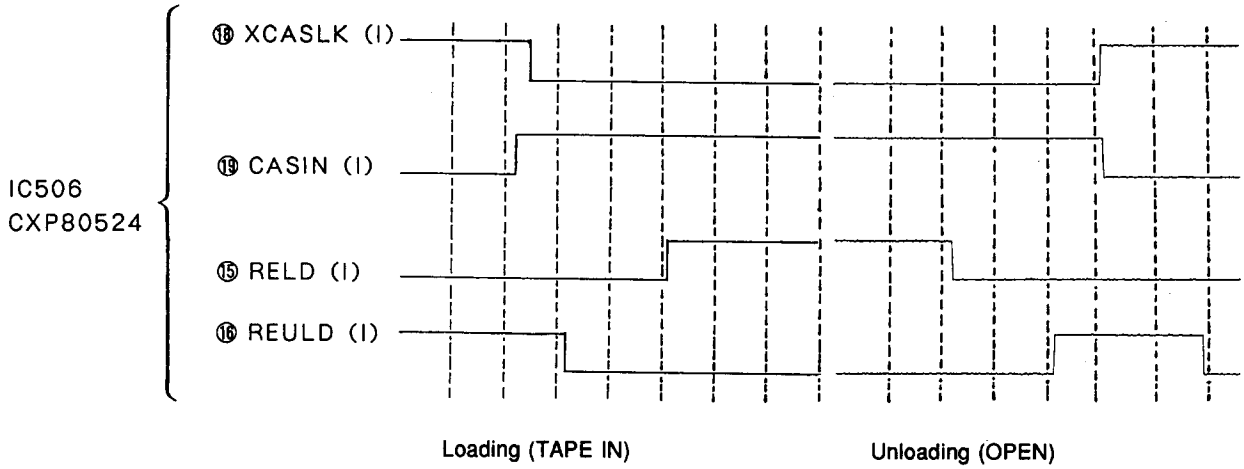


Fig. 7-6. Loading/Unloading Waveform Timing (500 ms/div)

7-3. Rotary Encoder and Mode Position Detection

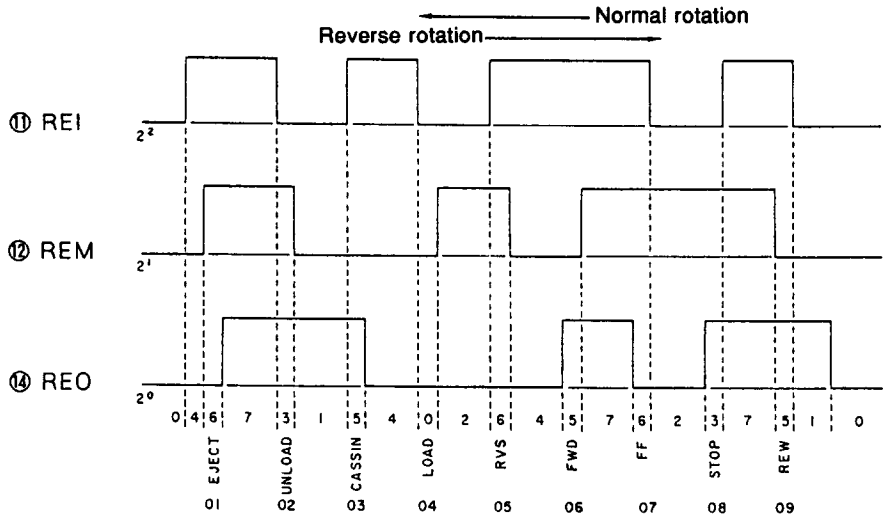


Fig. 7-7. Rotary Encoder Patterns

The rotary encoder (Part name:Cam gear (A)) is driven by the mode motor via the four relay gears. It is used to set the nine mechanism modes from EJECT to REW shown in **Fig. 7-7**. It controls the position of the encoder by controlling the mode motor according to the setting mode signal output from the mechanism controller. The rotary encoder is composed of a sliding element with four contacts attached to the rear of the cam gear (A) and electrode patterns shown in **Fig. 7-8**. By sliding on the COM pattern to which +4V power is supplied and REI to REO patterns cyclically, it identifies and controls the position of the encoder according to the combination of the outputs corresponding to which pattern exists. In the example shown in **Fig. 7-9** where the mode shifts from FWD to STOP, first the mode motor is rotated in the reverse direction (cam gear (B) rotates in the counterclockwise direction), and when the encoder detects the STOP position where REI is "L", REM is "H", and REO is "H", the mode motor stops via the brake mode. While the encoder is detecting the position, if it overruns and exceeds the target position, the mode motor is rotated in the reverse direction by pulse driving to shift to the correct position.

If the target position cannot be detected 5 seconds after the start up of the mode motor, it is determined as error, and an error code between "01 and 09" corresponding to the error is displayed on the LCD (for details, refer to the "Error Code Table" in the service manual".

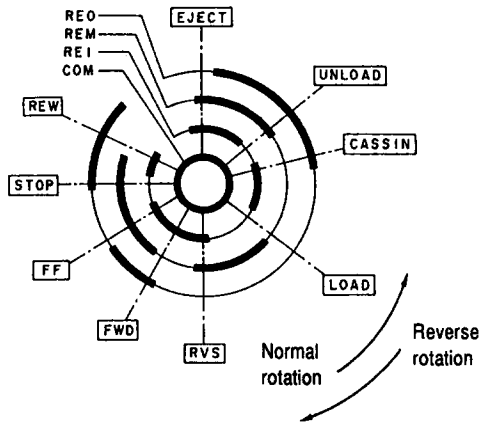


Fig. 7-8. Electrode Patterns of the Rotary Encoder (Rear View of Mechanism Deck)

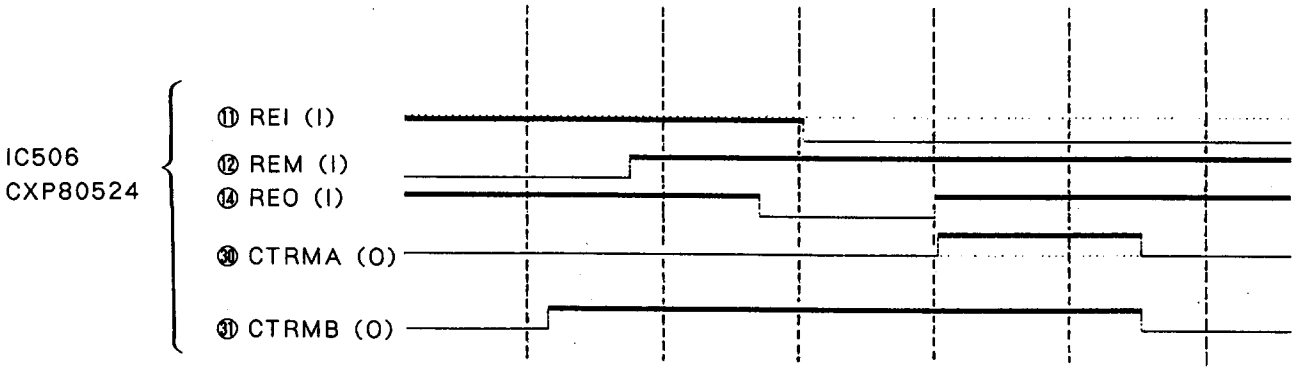


Fig. 7-9. Rotary Encoder Waveform Timings (FWD to STOP) (100 ms/div)

8. OPERATIONS OF MECHANISM

Note) The mechanism and the operations of this unit are the same as those of the TCD-D3/D7.
For details, refer to the "TCD-D3 Circuit Operations Guide".

8-1. Brake and Cam Gear (B) of Mechanism

The mechanism of this unit as shown in **Fig. 7-2** "Main Parts of Mechanism Deck" sets the mechanism modes using the mode motor and performs the driving of the T and S reel tables and loading/unloading of the tape running system using the capstan motor. The mode motor drives the cam gear (B) at the front of the mechanism deck and the rotary encoder (cam gear (A)) at the rear. The cam gear (B) controls the brake of the T and S reel tables and tension lever (lever (tension regulator)). **Fig. 8-1** shows the positions of the brake and tension lever used for the T and S reel tables of the unit's mechanism deck, and **Table 8-1** shows the main uses of these parts.

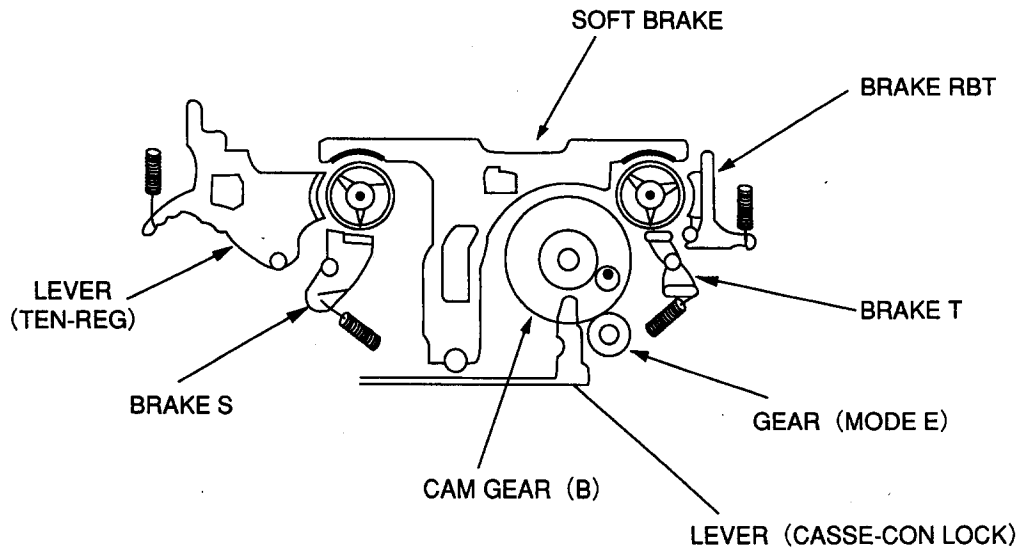


Fig. 8-1. Positions of Brake and Tension Lever

Table 8-1. Uses of Brake and Tension Lever

	Uses
Brakes S, T	Brakes used for stopping the reel tables in STOP mode, etc.
Soft brake	Brakes used for stabilizing tape running in FF/REW, AMS modes
Lever (Tension regulator)	Controls so that the back tension which changes according to reel diameter becomes constant in FWD (REC) mode
Brake RBT	Adds back tension to T reel table so that tape running stabilizes in RVS (reverse) mode

The cam gear (B) also controls the brake and tension lever, and also pinch roller compression. There are ribs (protrusions) at the front of this cam gear, whose positions are used to determine the positions of the mechanism as shown in **Fig. 8-2.** Their positions consist of nine positions from ① EJECT to ⑨ REW which are controlled by the rotary encoder. **Table 8-2** shows the operations of the brake and capstan motor at these positions. In the UNLOAD and LOAD modes, the T reel table operates while the brake and capstan motor are operating and locks T reel table using the T lock lever of the reel table assembly so that the tape does not slack.

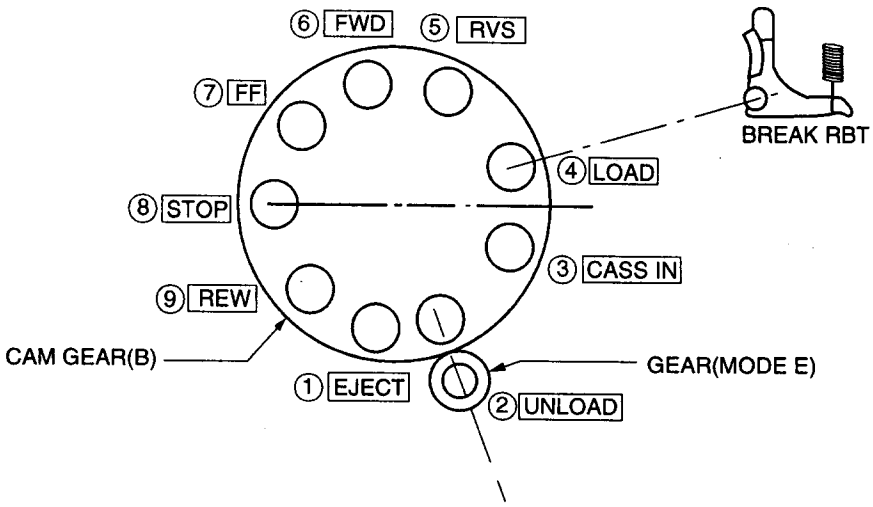


Fig. 8-2. Positions of Cam Gear (B) Ribs at Each Position

Table 8-2. Operations of Brake and Capstan Motor

Position	Brakes T and S	Soft Brake	Tension Lever	Brake RBT	Capstan Motor
① EJECT	O	O	X	X	–
② UNLOAD	X	O	X	X	x3RVS
③ CASSIN	O	O	X	X	–
④ LOAD	X	O	X	X	x3FWD
⑤ RVS	X*1	X	X	O	x3RVS (REV)
⑥ FWD	X	X	O	X	x1FWD*2
⑦ FF	X*1	O	X	X	*3
⑧ STOP	O	O	X	X	–
⑨ REW	X*1	O	X	X	*3

O: Operates X: Release
RVS: Reverse REV: Review
FWD: Forward
*1: Plunger maintains release state
*2: LP mode:x0.5 FWD, CUE mode:x3 FWD
*3: x25 to x100 (FF mode:FWD, REW mode:RVS)

8-2. Timing of Shift to Modes

1. Power Supply

When batteries are loaded or the AC adapter is connected without any cassette inserted, unloading is performed only once to reset the mechanism. When power is supplied, the rotary encoder is shifted from the position at this point to the UNLOAD mode to perform unloading, then shifted to the CASSIN mode, before stopping.
The rotary encoder operates as follows.

Position when power is supplied→UNLOAD→CASSIN

2. EJECT

When the power is supplied and EJECT (OPEN) is carried out without any cassette inserted, the cam gear (B) rotates from the CASSIN to EJECT position. As a result, the cassette holder opens, and the cassette control lock switch (S1002) turns on. After that, the cam gear (B) returns to the CASSIN position again.

CASSIN→EJECT→CASSIN

3. Cassette IN →STOP

After EJECT operations, when the tape is loaded with the cassette holder opened, and the holder is closed, the cassette IN switch (S1001) turns on, the cassette control lock switch (S1002) turns off, and the cam gear (B) shifts from the CASSIN to LOAD positions. The capstan motor rotates in the x3 FWD mode, and the tape running system performs loading. Following this, the cam gear (B) shifts to the RVS position, the tape runs in the x16 RVS mode for one second, and the main ID and sub code, etc. are read.
The cam gear (B) then shifts to the FWD position, and reverses in the x16 FWD mode to the position for completing loading. Following this, the cam gear (B) operates to the STOP position to complete shifting. The rotary encoder operates as follows.

CASSIN→LOAD→RVS→FWD→STOP

4. STOP →FWD

Shifting to the FWD mode is completed when the FWD position is detected by the encoder.
As a result, the FWD mode mechanism settings are performed such as pressing the pinch roller, releasing T and S brakes, etc., and the capstan motor starts rotating.

STOP→FWD

5. STOP →FF/REW

To shift to the FF or REW mode, first the rotary encoder is operated to this mode once to draw the plunger. After this, the encoder is rotated to the STOP position again to complete shifting. At this time, the plunger maintains the brake release state of both reel tables. The rotation of the capstan motor is started immediately after the encoder is returned from the FF or REW position to the STOP position.
To shift from the FF or REW mode to the STOP mode, the plunger stops maintaining the brake T and S release state, and promptly stops the rotation of the reel table.
The encoder operates as follows when shifting to the FF/REW modes.

STOP→FF/REW→STOP (In this state, the brake of the reel table is released by the plunger, and FF/REW operations are performed.)

6. STOP →EJECT

To shift the mode when ejected in STOP mode, first the rotary encoder is moved to the UNLOAD position, and after the mode has been shifted, the capstan motor is rotated in the x3 RVS mode to unload. After this the rotary encoder is shifted to the EJECT position. The operations after this are the same as EJECT.
(Refer to 2.EJECT.)

STOP→UNLOAD→EJECT→CASSIN

7. FWD →STOP

The shift to the STOP mode is ended when the rotary encoder is detected to be at STOP position.
The capstan motor stops at the same timing as the start up of the mode motor.

FWD→STOP

8. REC/REC PAUSE→STOP

The mechanism is in the FWD state in the REC or REC PAUSE mode. When the mechanism is shifted from this mode to STOP, in order to ensure a tag recording, the mechanism mode is shifted to RVS before shifting to the STOP mode, and after, the tape is returned in the x1 RVS mode for one second, the mechanism is shifted to the STOP mode.

FWD→RVS→STOP

9. FWD →x25 FWD (High speed CUE)

In the high speed CUE mode, the mechanism is driven in the FF mode, but the mechanism is not directly driven from FWD to FF, but to the STOP position once to impose a mechanical brake, before shifting to the FF mode. The operations after this are the same as STOP →FF.
(Refer to 5. STOP→FF.)

FWD→STOP→FF→STOP (The brake of the reel table at this time is released by the plunger, and FF operations are carried out.)