Catalog No. 1809670-01
Issued: August 1985

TBC-6

DIGITAL TIME-BASE CORRECTOR (PAL)

SERVICE MANUAL

AMPEX

Prepared by

AVSD Technical Publications
Ampex Corporation
401 Broadway
Redwood City, CA 94063

Catalog No. 1809670-01
Issued: August 1985

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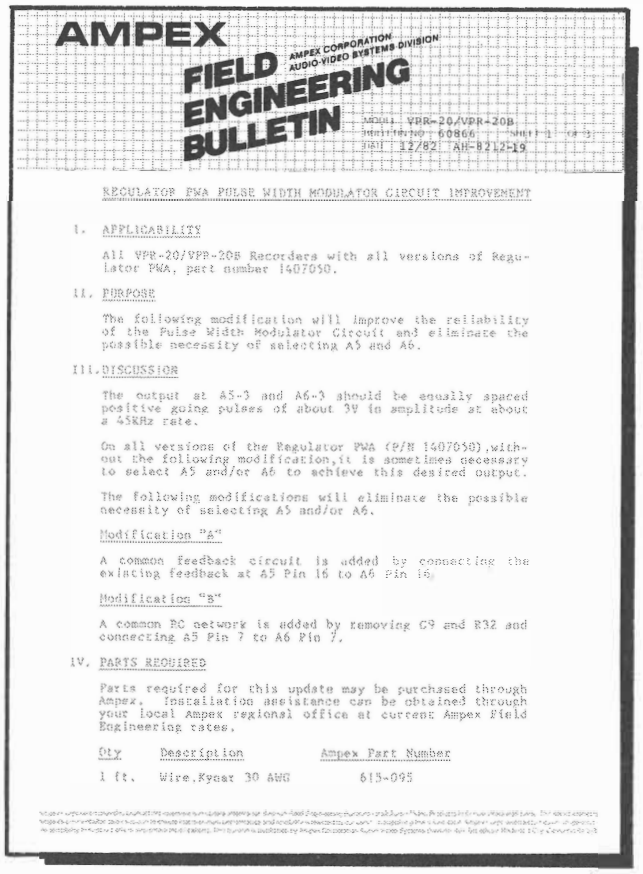

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AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

FIELD ENGINEERING BULLETIN

MODEL VPR-20/VPR-20B
BULLETIN NO 60866 REV 1
DATE 12/82 AH-8212-19

REGULATOR PWA PULSE WIDTH MODULATOR CIRCUIT IMPROVEMENT

I. APPLICABILITY

All VPR-20/VPR-20B Recorders with all versions of Regulator PWA, part number 1407050.

II. PURPOSE

The following modification will improve the reliability of the Pulse Width Modulator Circuit and eliminate the possible necessity of selecting A5 and A6.

III. DISCUSSION

The output at A5-3 and A6-3 should be equally spaced positive going pulses of about 3V in amplitude at about a 45KHz rate.

On all versions of the Regulator PWA (P/N 1407050),without the following modification,it is sometimes necessary to select A5 and/or A6 to achieve this desired output.

The following modifications will eliminate the possible necessity of selecting A5 and/or A6.

Modification "A"

A common feedback circuit is added by connecting the existing feedback at A5 Pin 16 to A6 Pin 16.

Modification "B"

A common RC network is added by removing C9 and R32 and connecting A5 Pin 7 to A6 Pin 7.

IV. PARTS REQUIRED

Parts required for this update may be purchased through Ampex. Installation assistance can be obtained through your local Ampex regional office at current Ampex Field Engineering rates.

Qty	Description	Ampex Part Number
1 ft.	Wire,Kynar 30 AWG	615-095

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Serial No.
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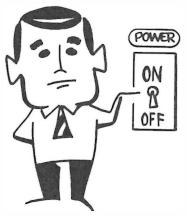
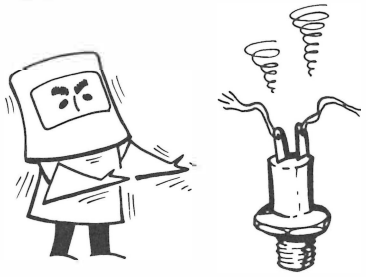
SAFETY AND FIRST AID SUGGESTIONS

Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:



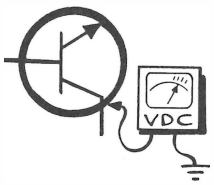
1 Do not attempt to adjust unprotected circuit controls or to dress leads with power **on.**



2 Do not touch heavily loaded or overheated components without precaution to avoid burns.

3 Do not assume that all danger of electrical shock is removed when power is **off.** Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

4 Always avoid placing parts of the body in series between ground and circuit points.



5 Remember that some semiconductor cases and solid-state circuits carry high voltages.

6 Don't take chances. Be fully trained. Ampex equipment should be operated and maintained by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT TOUCH VICTIM OR HIS CLOTHING BEFORE POWER IS REMOVED OR YOU MAY ALSO BECOME A SHOCK VICTIM.

If power cannot be removed immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

GOOD PRACTICES

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

1. When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.

2. When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

3. When troubleshooting, remember that FETs and other metal-oxide-semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

4. When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

5. When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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TBC-6 Digital Time-Base Corrector

SECTION 1
GENERAL INFORMATION

1-1 INTRODUCTION

This manual provides information necessary to operate and maintain the PAL version of the TBC-6 Digital Time-Base Corrector (DTBC), Ampex Part No. 1451605.

This section is an introduction to the TBC-6, its features and system specifications. Section 2, *Theory of Operation*, gives operating theory for the system in general and for each PWA to the block diagram level. Section 3 lists procedures for aligning circuits in the system. Section 4, *Removal and Replacement*, gives procedural instructions for replacing major assemblies of the TBC-6. Section 5, *Supplemental Information*, contains detailed lists which supplement maintenance information. Section 6 provides jumper location diagrams for each PWA in the TBC-6.

1-2 RELATED PUBLICATIONS

The following publications contain information related to TBC-6 service, and should be referred to as required:

- TBC-6 Installation and Operation, Catalog No. 1809643
- TBC-6 Parts Lists and Schematics, Catalog No. 1809647

1-3 GENERAL DESCRIPTION

The following paragraphs describe some of the features, functions, and physical aspects of the system.

1-4 Features

The TBC-6 Digital Time-Base Corrector affords correction over a 28-line window, slow-motion processing to 1-1/2X forward when used with the Ampex VPR-6, and recognizable pictures in shuttle to 500 in/s. The TBC-6 also provides dropout replacement from two lines away without horizontal shift.

The TBC-6 motherboard, which provides interconnection for the plug-in PWAs, features a unified bus structure, which permits individual PWAs to be inserted in any position. This allows a PWA under test to be inserted in the top position for access to the component side during fault isolation or alignment. While servicing the PWA inserted in the top position, the Video Input PWA is inserted in the position used by the board under test. The TBC-6 functions normally in this configuration and allows access to components while operating.

1-5 Functional Description

The TBC-6 receives off-tape video from nonsegmented helical-scan videotape recorders. The off-tape video signal is sampled at four times subcarrier frequency by a sampling clock signal derived from the burst frequency of incoming off-tape video. The resulting analog video sample goes to an analog-to-digital converter which converts the instantaneous video level to an 8-bit binary number corresponding to the level at the time of the sample. Digital data is written sequentially into memory synchronous with off-tape timing. Stored data is subsequently read out of memory in the same sequence as it is written. Read timing is derived from reference video and output data is synchronous with reference video. Eight-bit data read-out of memory is converted to an analog level by a digital-to-analog converter. The converted analog signal is filtered to provide a video signal. Blanking and sync are inserted in the resultant video to form the composite video output signal.

1-6 Physical Description

The TBC-6 is a self-contained unit that may be mounted in a table-top cabinet, a VTR console, or rack mounted. Electronic circuits are contained on four individual printed wiring assemblies (PWAs) which plug into a motherboard PWA. Table 1-1 is a list of individual PWAs and their Ampex part numbers. TBC-6/VTR interface connectors are located at the rear of the cabinet and are mounted directly on the Motherboard PWA.

Table 1-1. TBC-6 Printed Wiring Assemblies

Printed Wiring Assembly	Ampex Part No.
A1 Video Input PWA	1451652
A2 Tape Clock PWA	1451655
A3 Memory System PWA	1451750
A4 Video Output PWA	1451753

1-7 TYPICAL APPLICATIONS

The TBC-6 is a compact, high-performance time-base corrector for use with C-, M-, and U-format VTRs. The TBC-6 is an ideal companion to the Ampex VPR-6 Video Production Recorder. The TBC-6 has switch-selectable video inputs to allow it to be used with C-format and U-format (3/4 in.) or M-format (1/2 in.) VTRs when dubbing from two sources. Figure 1-1 shows a typical TBC-6 system application.

1-8 SPECIFICATIONS

Specifications and performance characteristics of the TBC-6 are listed in Table 1-2. These specifications are subject to change without notice or obligation.

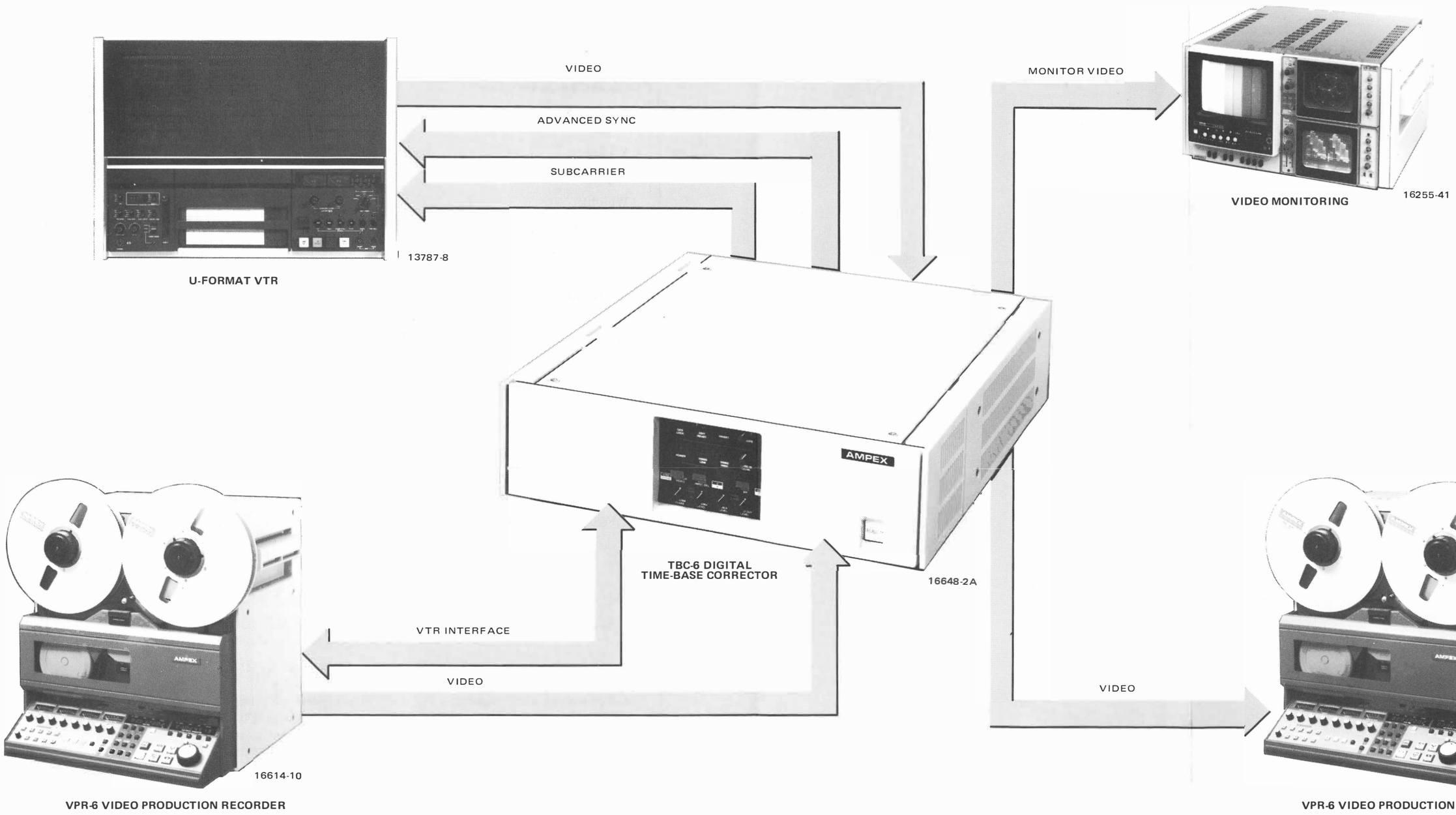


Figure 1
Typical TBC-6 System Configurat

Table 1-2. TBC-6 Specifications

Physical Characteristics	
Height:	(133 mm) 5.25 in.
Width:	(500 mm) 19.7 in.
Depth:	(549 mm) 21.625 in.
Weight:	(18 kg) 40 lb
Operating temperature:	(0° to +40° C) 32° to 104°F
Operating humidity:	10% to 90% relative (noncondensing)
Power Requirements	
Input Power:	50 Hz to 60 Hz, single phase, 150W 90 Vac to 140 Vac or 190 Vac to 250 Vac
System Interface	
VTR video in A and B:	1 Vp-p, 75Ω
Reference video in:	1 Vp-p, high-impedance, loopthrough connectors
RF dropout input:	0.1V to 2.0V
C-Format VTR interface signals:	Step back, step back 2, sync retard, playback vertical, fast shuttle, edit mute, slow-motion, dropout pulse, head switch/vertical dropout, 2H gate, step forward sync head process, zero offset.
Video out 1:	1.0 Vp-p composite 75Ω
Video out 2:	1.0 Vp-p composite 75Ω 0.7 Vp-p noncomposite 75Ω
Monitor video output:	1.0 Vp-p composite 75Ω
Advanced reference output:	VTR advanced reference: color black, composite sync at video levels (75Ω) or sync/vertical drive at −4V level, jumper selectable.
Sync coherent subcarrier output:	1V subcarrier, 75Ω
Operational Characteristics	
Bandwidth:	Flat to 4.2 MHz, ±0.2 dB

(Continued next page)

Table 1-2. TBC-6 Specifications (Continued)

Operational Characteristics (Continued)	
Signal-to-noise ratio (1):	56 dB
Differential phase (2):	2°
Differential gain (2):	2%
Transient response (2T pulse and bar):	1% K factor
Correction range:	28 horizontal lines
Output jitter:	±3 ns color; ±20 ns monochrome

(1) VTR-TBC system signal-to-noise ratio is determined primarily by VTR performance.

(2) Defined as the degradation to the differential gain of the input video signal, measured with ramp and subcarrier amplitude equal to that of the color burst.

SECTION 2
THEORY OF OPERATION

2-1 INTRODUCTION

This section describes TBC-6 functional operation and interrelation of PWAs in the system. Also included are block diagrams of the overall system and individual PWAs that comprise the system.

2-2 GENERAL DESCRIPTION

Time-base correction compensates for timing errors introduced when video signals are recorded on magnetic tape. A video tape recorder is a complex electro-mechanical device. In spite of care in design and manufacture, it is impossible to avoid generating mechanically induced errors, particularly when the recorder is not the same unit used for playback. In addition to timing variations caused by wow, flutter, speed, gyroscopic effects, and velocity errors between recorder/reproducers, tape length varies because of temperature differences and mechanical stresses. The result of all of these errors is mistiming of the video signal at the video tape recorder output. Depending on the amount of mistiming, these errors appear in the final picture as a change in color, horizontal position, vertical position, or a combination of the three.

TBC-6 time-base correction is accomplished in two stages. First, tape burst crossing locks a VCO that generates a tape 4Fsc (four times the 4.45-MHz subcarrier, or 17.7 MHz) signal which is used to digitize the analog video signal. Due to timing errors discussed in the previous paragraph there may be as much as a 40° phase error between tape burst crossing and the tape 4Fsc signal. The tape burst crossing to tape 4Fsc error (line-by-line) is measured and stored in memory with the digitized data from each particular line, using the tape 4Fsc clock. The line-by-line error is read out of memory by a reference 4Fsc developed in the sync generator from the reference (station) burst crossing. This error data is routed to the time-base error profile generator which reconstructs the line-by-line error signal and performs a linear interpolation of this signal. This linear interpolation develops a time-base error signal that represents both line-by-line error and velocity error. The reference 4Fsc is then modified by this time-base error signal within the phase modulator and becomes the read 4Fsc clock. The second stage of time-base correction is then performed in the D/A by converting the digital video to analog using the read 4Fsc clock.

The TBC writes video picture information into memory at a tape 4Fsc rate on a line-by-line basis. The video picture information is read out of memory at the reference 4Fsc rate. Reference sync and burst are then added to the picture information to to create a stable video picture.

The TBC-6 Digital Time-Base Corrector affords correction over a 14-line window, slow-motion processing to 1-1/2X forward when used with the Ampex VPR-6, and recognizable pictures in shuttle to 300 in/s. In addition to a choice of two processed video outputs (VIDEO 1 and VIDEO 2) at the rear of the TBC, a monitor output, fed from a monitor amplifier, will supply either processed TBC video or the selected input video.

2-3 TBC-6 SIMPLIFIED BLOCK DIAGRAM DISCUSSION

The primary functional breakout of the TBC system is input processing, output processing, time-base error processing, and storage. Referring to the system simplified block diagram (Figure 2-1), note that the 32-line memory storage is in the center. The input processing group consists of the video input, color processor, and video A/D converter, while the output processing group consists of the video output and the sync generator. The time-base error processing group consists of the tape clock and the memory control.

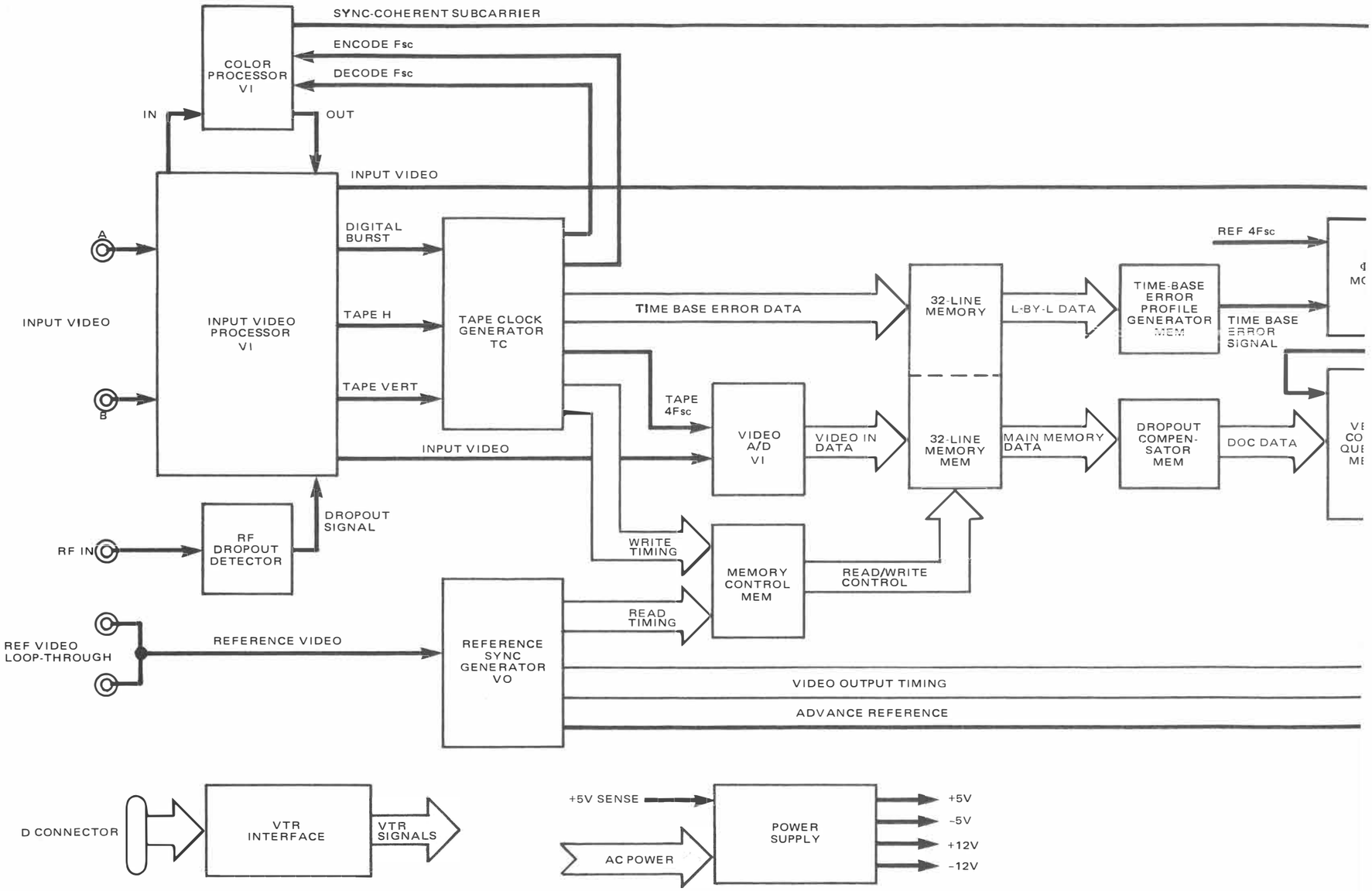
Off-tape video is received by the input video processor, which clamps and amplifies the signal, switches the signal through the color processor circuits, switches off-tape or TBC video to the monitor video output, and strips burst and sync information from the off-tape video signal for use by the tape clock generator. These circuits also provide input video level monitoring with a video high/low warning on the control panel.

The color processor permits the TBC to be used with the VPR series in slow-motion mode and also allows the TBC to be used with a heterodyne-type color VTR. In order to maintain the proper PAL sequence in slow motion, the color processor on the Video Input PWA must decode the chrominance into its U and V components. The chrominance is then reencoded with a sync-coherent subcarrier, reestablishing the proper color frame. In heterodyne this same operation establishes a coherency between input video sync and subcarrier.

The A/D converter quantizes the off-tape video into a binary digital representation of the video's instantaneous voltage level at a conversion rate of tape 4Fsc. Each binary digital representation consists of an 8-bit data word. The data is stored in memory at the basic clock rate (tape 4Fsc).

The Tape Clock PWA contains the tape VCO which generates the tape 4Fsc. The tape VCO is locked to a selected burst crossing. Measurement between the selected burst crossing and the tape 4Fsc is also accomplished (line-by-line error) and the results digitized and output to the Memory System PWA. During slow motion a decode Fsc is derived from input burst and used to decode chrominance and an encode Fsc is developed to reencode the chrominance components onto a new subcarrier in the color processor. The Tape Clock PWA also generates a write timing signal based on the tape 4Fsc oscillator output.

The Memory System PWA stores 32 lines of video. The memory acts as a buffer and, when there are no time-base errors, a line of video is read out of memory approximately eight lines after it has been written into memory, and memory is said to be centered.



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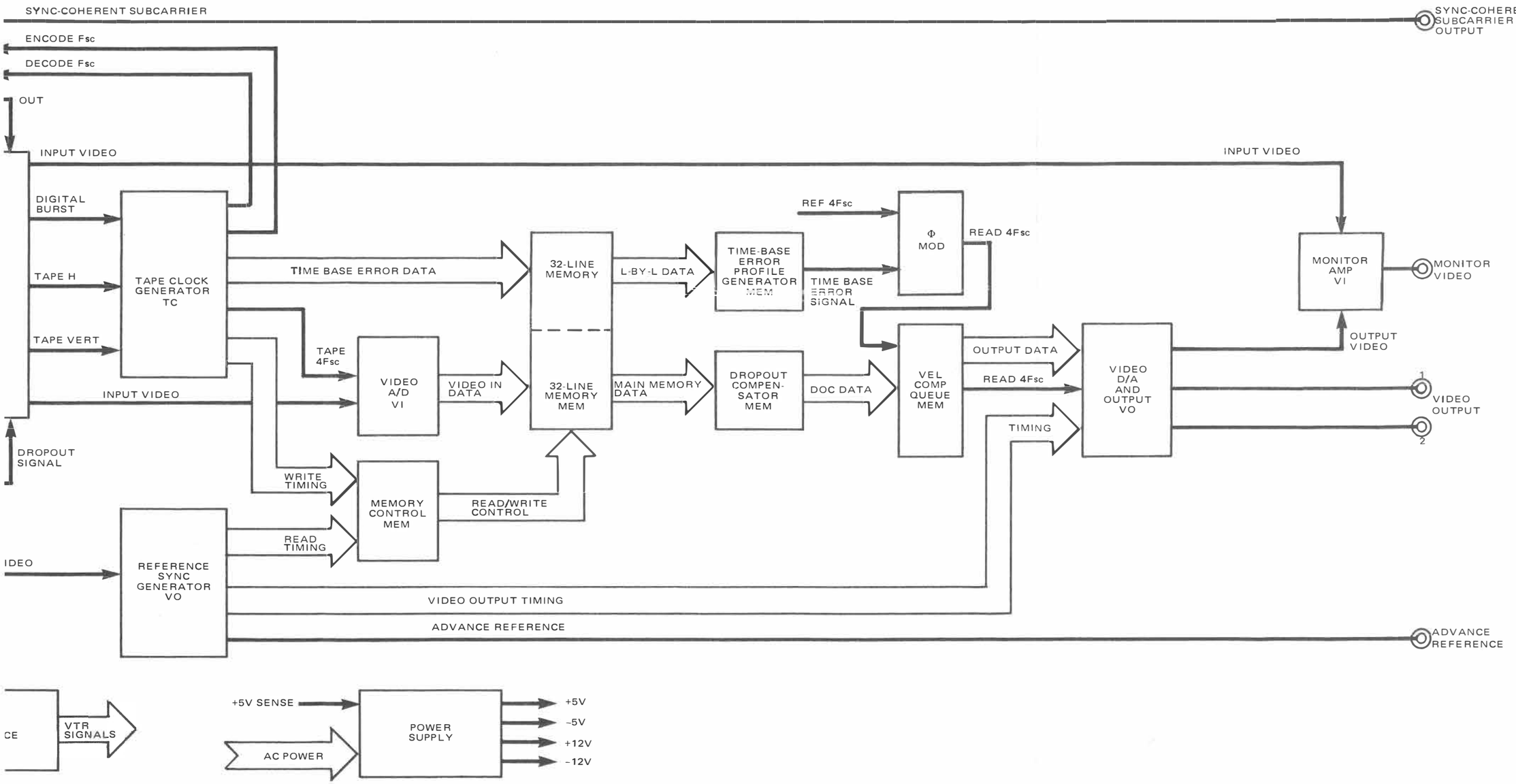


Figure 2-1.
Simplified Block Diagram.

Memory access signals are generated by the memory control circuits. These circuits also center read-write timing of the memory after the occurrence of time-base disturbances to ensure that the buffering capability of memory is optimized. Memory centering, in effect, refers to the vertical centering of the frame. To accomplish this, the write timing always uses as a reference the tape vertical. The read timing is always referenced to the reference vertical.

The PAL TBC-6 sync generator synthesizes both reference subcarrier and reference sync signals from a single oscillator. To do this, a three step process is involved.

- The first step is to phase-lock a reference 4Fsc oscillator to reference burst. This establishes a 4Fsc clock signal whose frequency represents the reference burst frequency. Because of the 25-Hz offset between sync and subcarrier frequencies in the PAL I system, the 4Fsc clock signal must be shifted down by 100 Hz before it can be used to generate composite sync signals.
- The second step thus involves the synthesis of an H-4Fsc signal (1135H) from the reference 4Fsc clock which is used to generate all of the reference H-related signals used on the Video Output PWA.
- The third step is a phase alignment between the reference Fsc and the output sync.

A two-line dropout compensator is provided on the Memory System PWA. The two-line dropout compensator manipulates the 8-bit data to supply replacement video (which is composite of luminance and inverted chroma extracted from two lines previous). This replaces the current data (dropout) from the output of memory during the time that a dropout is detected. Dropouts are identified by a TTL dropout signal originating in the VPR or a loss of rf signal from the VTR.

The line-by-line error data, from the 32-line memory, is routed to the time-base error profile generator where a linear interpolation of the line-by-line error signal is performed. This linear interpolation develops a time-base error signal that represents both line-by-line error and velocity error. The reference 4Fsc is then modified by this time-base error signal within the phase modulator and becomes the read 4Fsc clock.

In the video D/A and output circuits, the 8-bit words are converted back to an analog signal which, together with inserted sync burst and blanking information supplied by the sync generator, provides output video from the TBC.

Within the monitor amplifier, either input video (TBC input data) or output video (TBC processed video) is selected and routed to the monitor video output jack on the TBC back panel.

2-4 SIGNAL PROCESSING

See Figure 2-2. Video input to the TBC-6 is routed from the rear panel connectors to the Video Input PWA. In the Video Input PWA, either video A or video B is

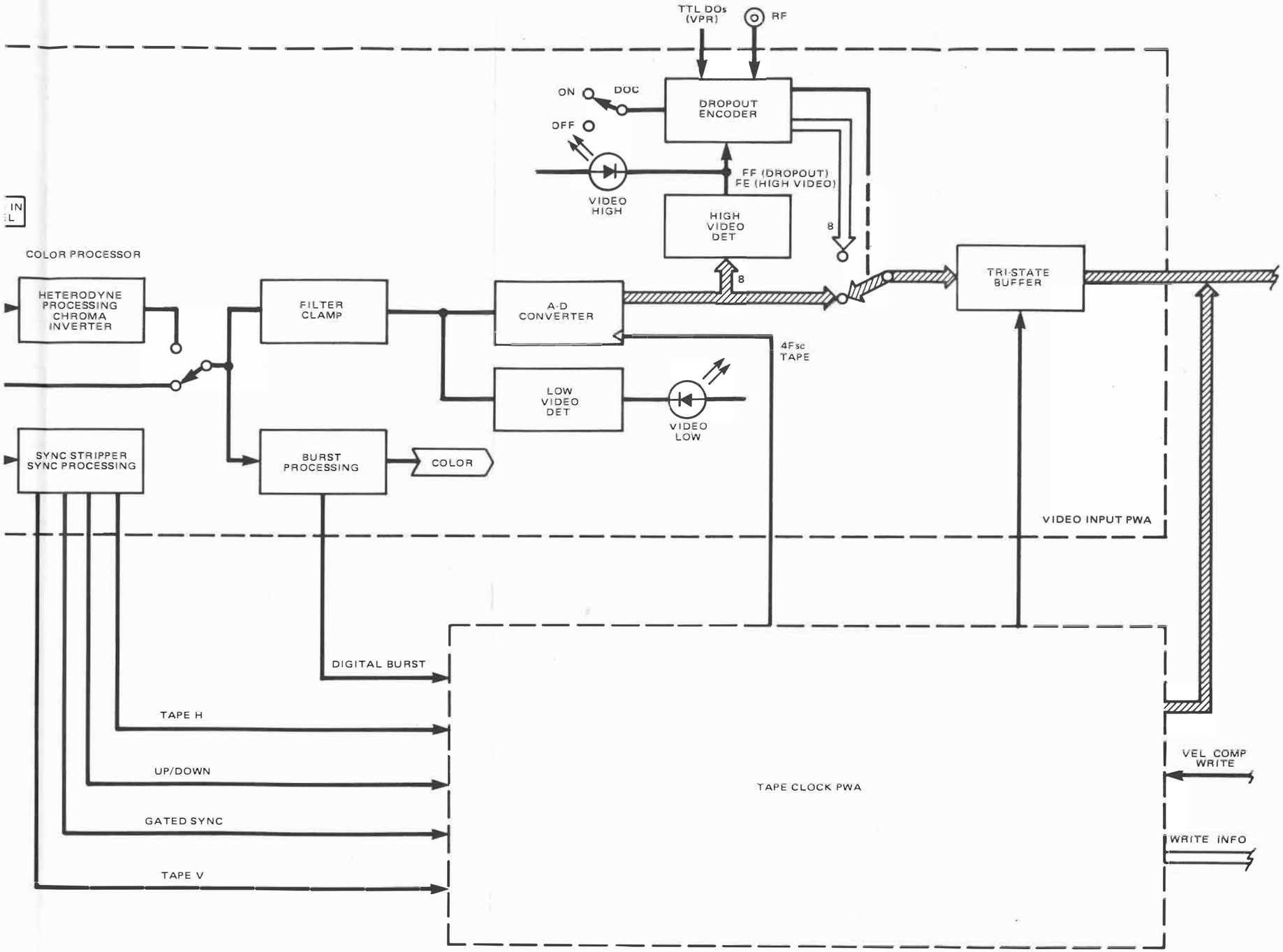
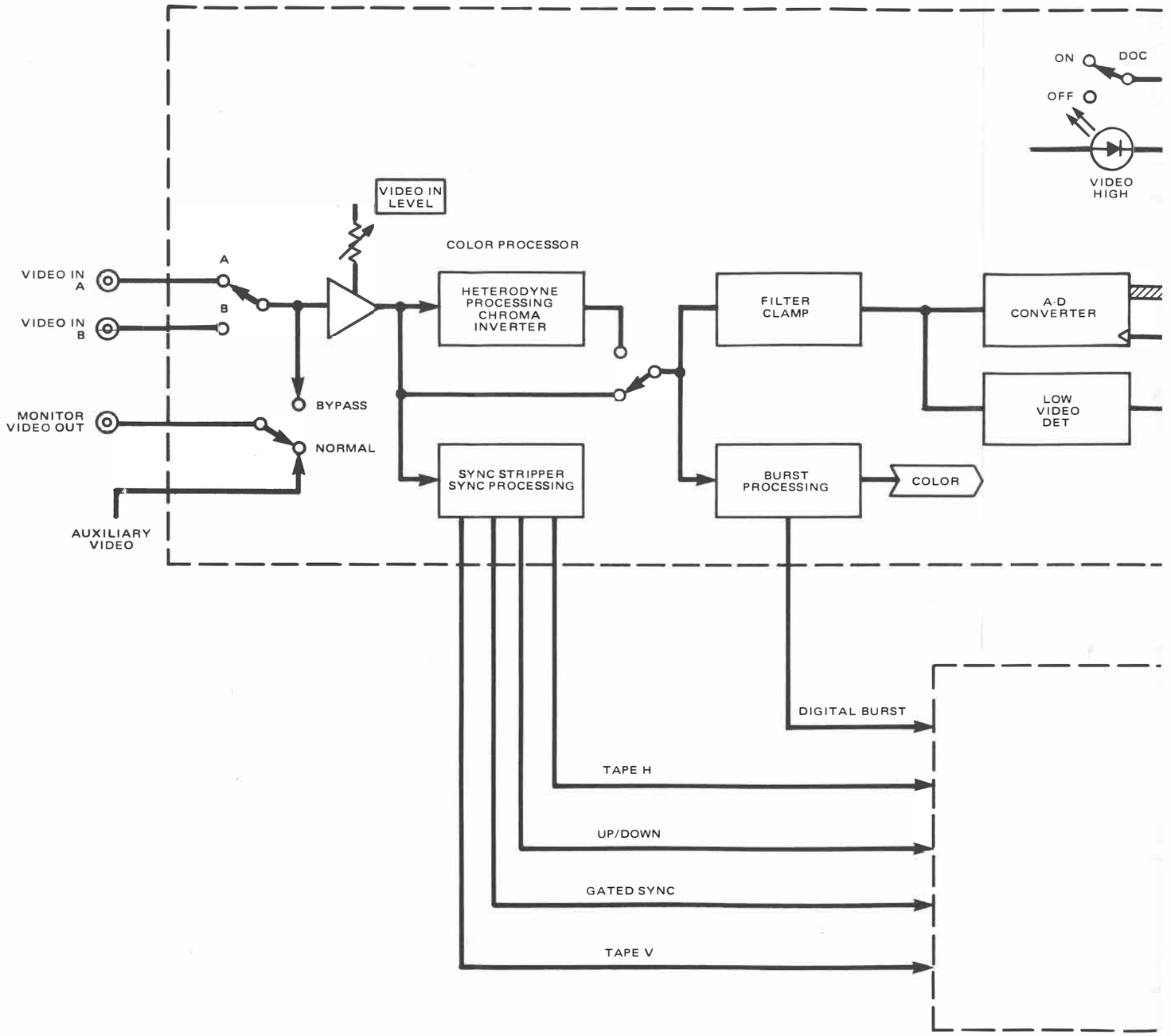


Figure 2-2.
TBC-6 Signal Flow, Block Diagram
(Sheet 1 of 2)



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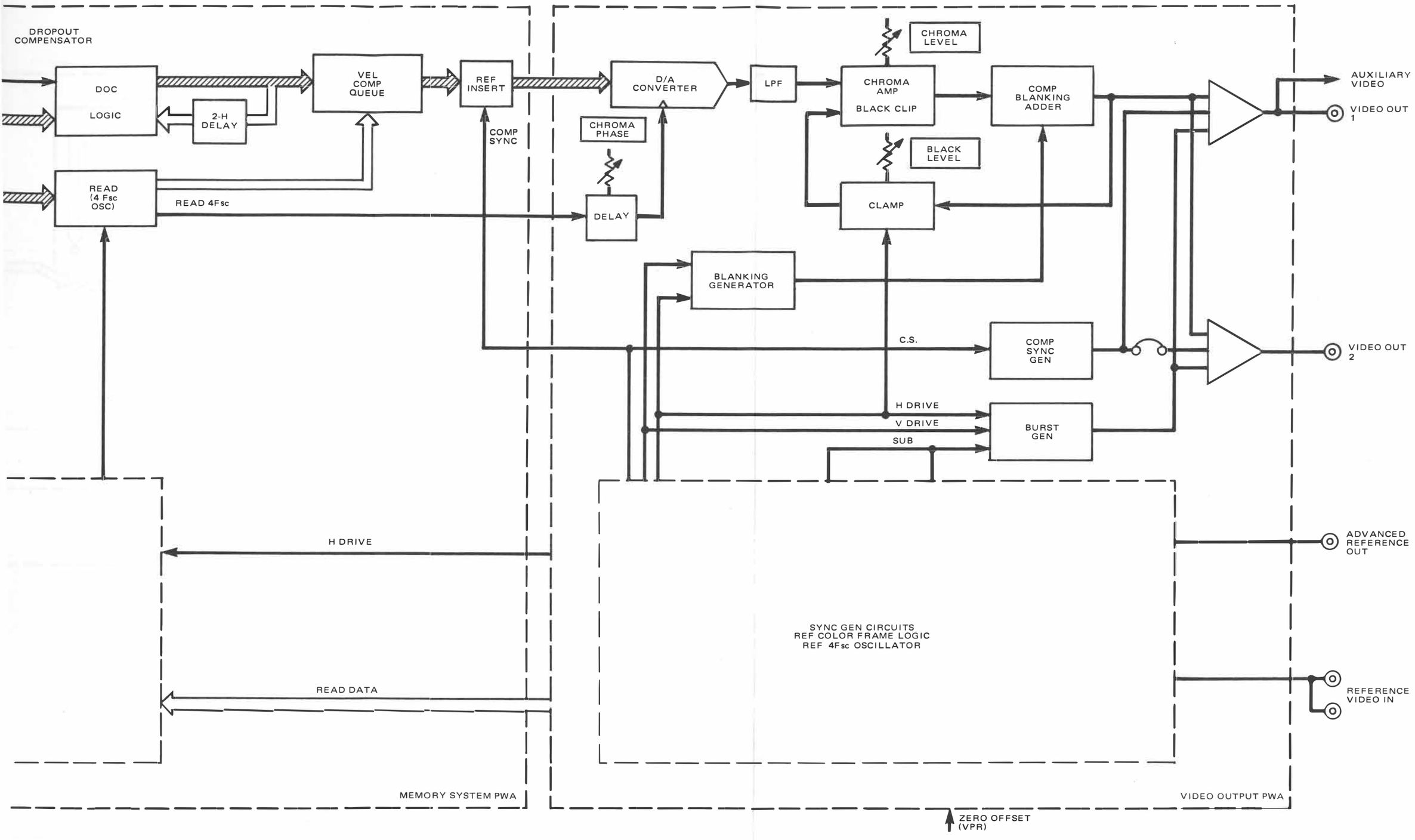
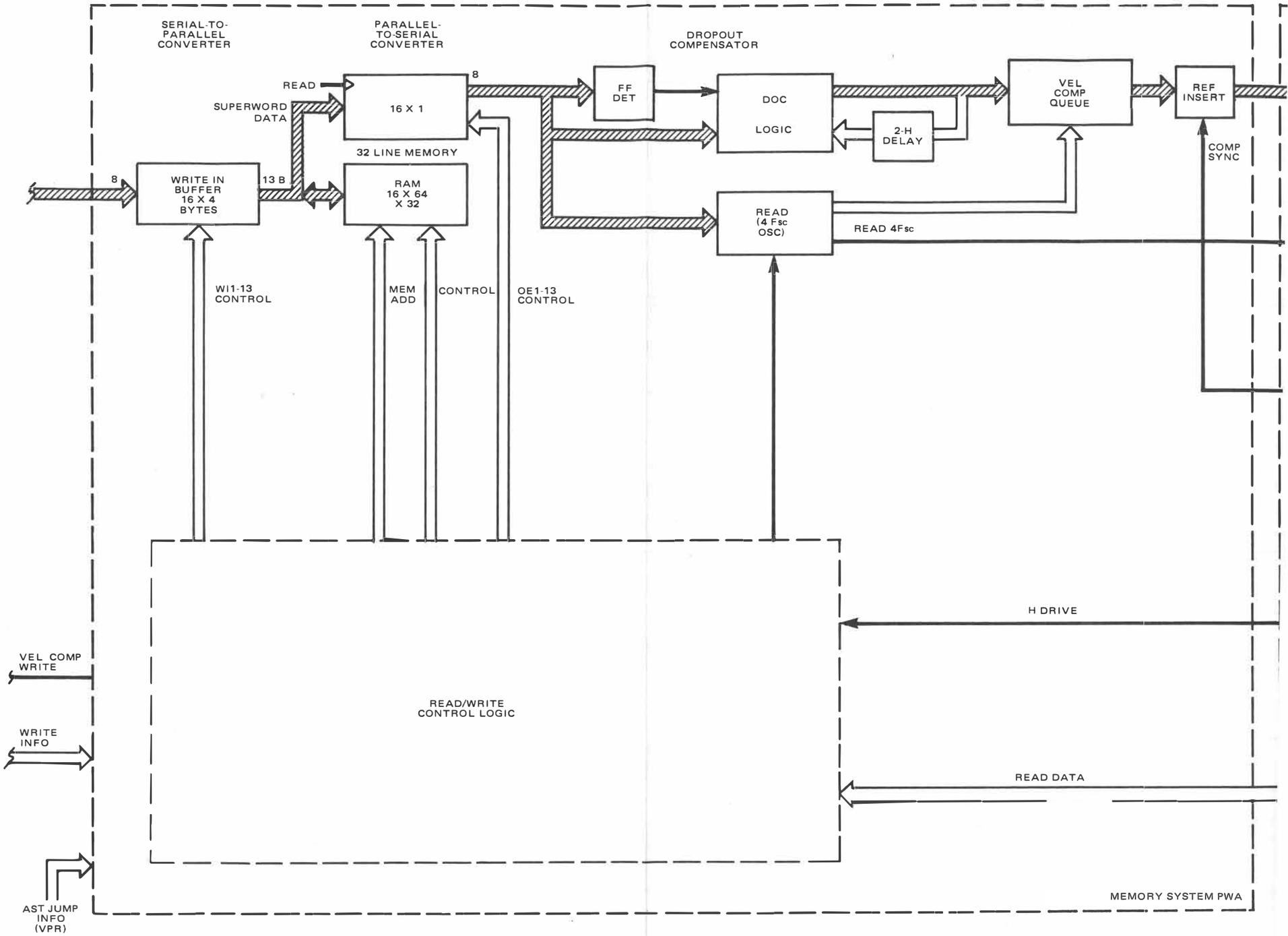


Figure 2-2.
TBC-6 Signal Flow, Block Diagram
(Sheet 2 of 2)


SERIAL-TO-PARALLEL CONVERTER
PARALLEL-TO-SERIAL CONVERTER
DROPOUT COMPENSATOR
READ
SUPERWORD DATA
16 X 1
8
FF DET
DOC
LOGIC
2-H DELAY
VEL COMP QUEUE
REF INSERT
COMP SYNC
32 LINE MEMORY
8
WRITE IN BUFFER 16 X 4 BYTES
13 B
RAM 16 X 64 X 32
READ (4 Fsc OSC)
READ 4Fsc
WI1-13 CONTROL
MEM ADD
CONTROL
OE1-13 CONTROL
H DRIVE
VEL COMP WRITE
READ/WRITE CONTROL LOGIC
WRITE INFO
READ DATA
AST JUMP INFO (VPR)
MEMORY SYSTEM PWA

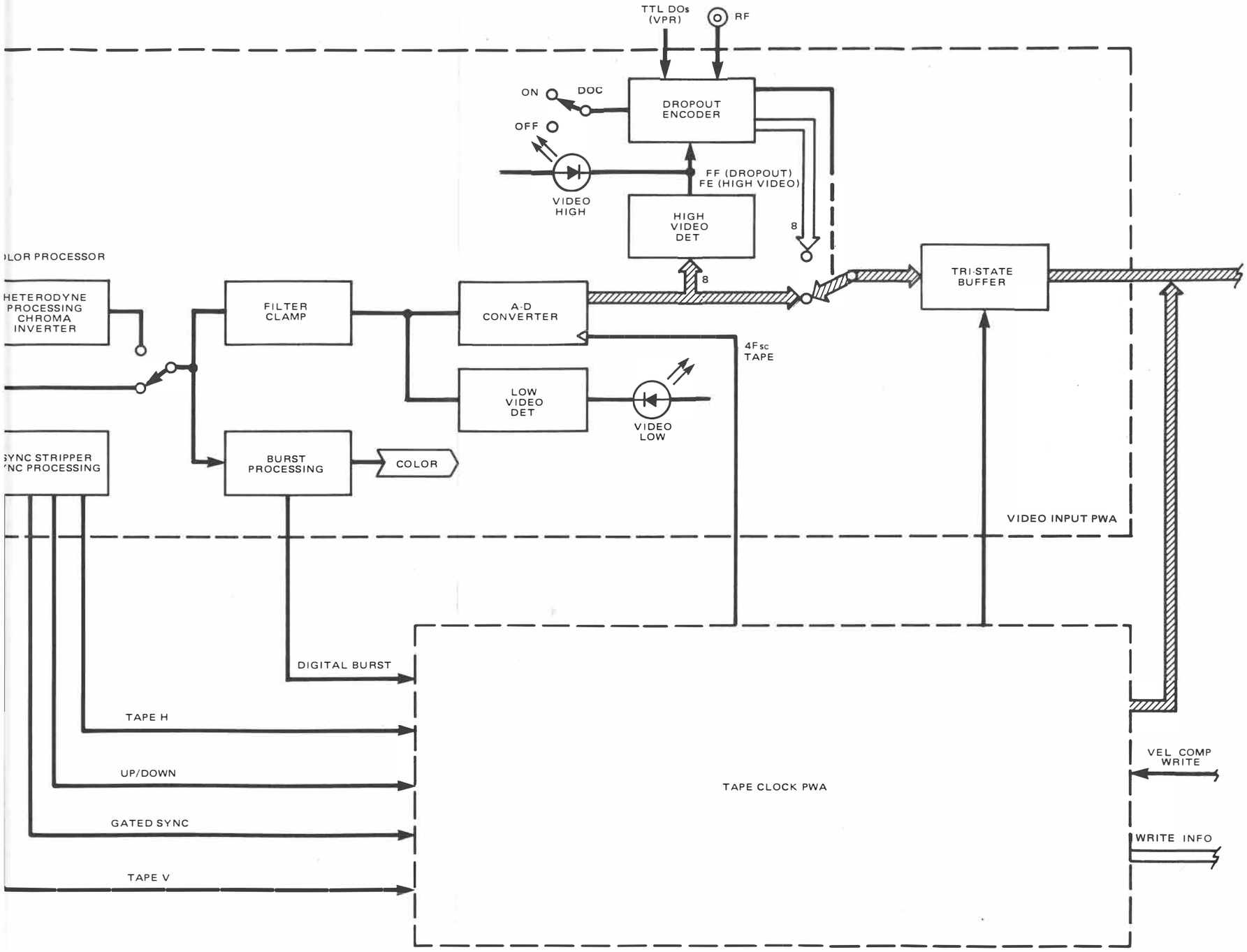
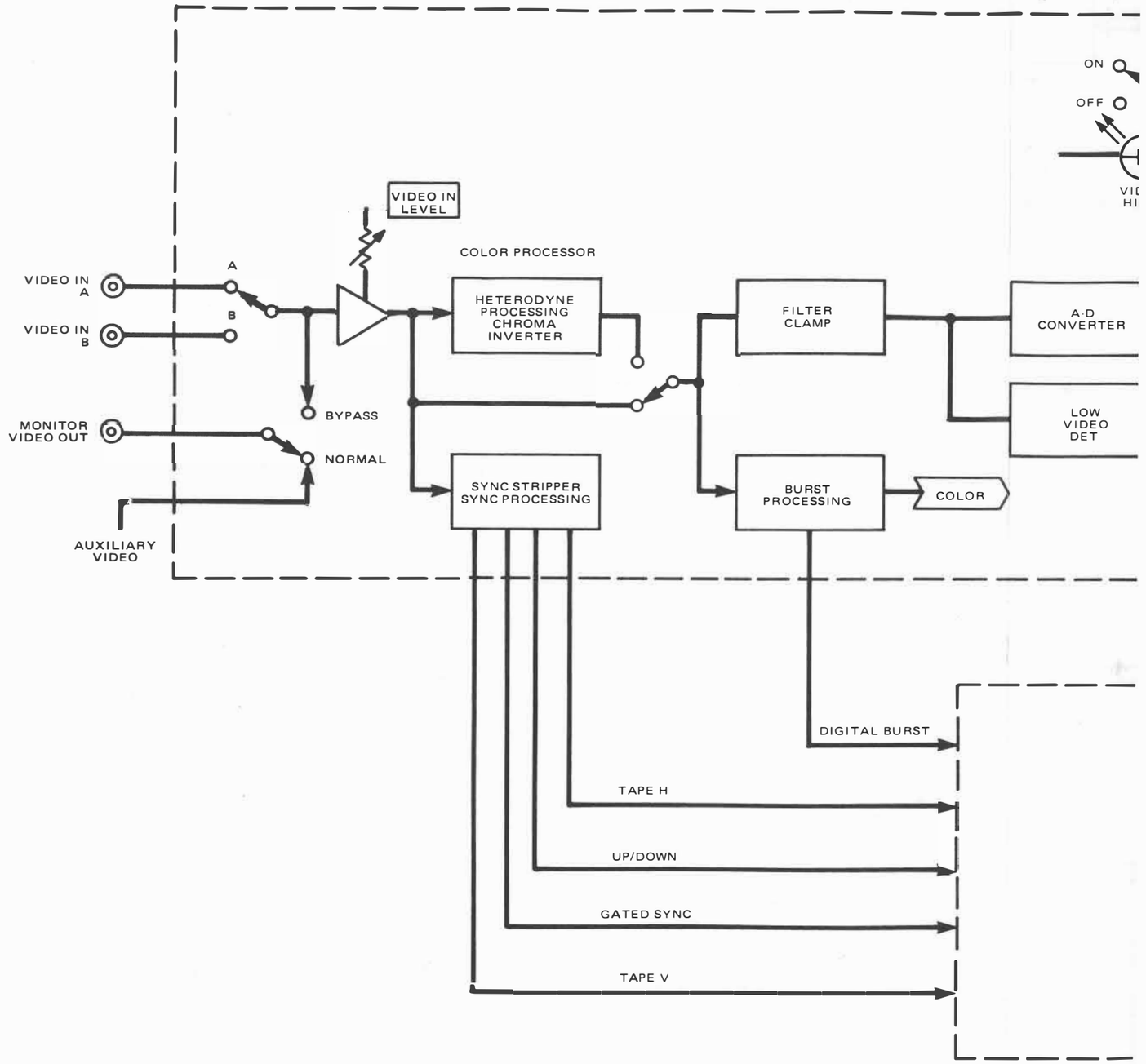


Figure 2-2.
TBC-6 Signal Flow, Block Diagram
(Sheet 1 of 2)


ON
OFF
VIDEO IN LEVEL
COLOR PROCESSOR
VIDEO IN A
VIDEO IN B
A
B
HETERODYNE PROCESSING CHROMA INVERTER
FILTER CLAMP
A-D CONVERTER
BYPASS
LOW VIDEO DET
MONITOR VIDEO OUT
NORMAL
SYNC STRIPPER SYNC PROCESSING
BURST PROCESSING
COLOR
AUXILIARY VIDEO
DIGITAL BURST
TAPE H
UP/DOWN
GATED SYNC
TAPE V

selected, amplified, and clamped. After amplification the video is sent to the sync stripper circuits, to the color processor (during slow motion or one-wire heterodyne operation), and to the A/D converter and burst processing circuits. The sync stripper circuits ensure that an authentic sync signal is used to generate the tape vertical, gated sync, up/down, and tape H signals that are sent to the Tape Clock PWA. Burst is detected and routed to the burst processing circuits to detect the presence of color and to digitize the burst signal for use in the Tape Clock PWA.

The filter clamp establishes a fixed back porch level for the TBC-6 and a reference level for the A/D converter. In the A/D converter the video is sampled, at a tape 4Fsc rate, converted and routed to the Memory System PWA. Dropout encoding circuits in the Video Input PWA insert an FF binary code on the video bus when a dropout signal is received from an external source. When an FF (A/D converter overload) is sensed by the high video detector circuits, the video-high lamp lights and a binary FE is routed through on the video bus. The video-low lamp lights when sync is low.

Digitized input video and digitized line-by-line error are multiplexed on this video bus. The tri-state buffer is disabled by the vel comp write signal from the memory read/write control logic during the time the tape clock is suppling the line-by-line error signal.

The digital video from the Video Input PWA and the tape 4Fsc error signal from the Tape Clock PWA are written into the write-in buffer on the Memory System PWA. Data is clocked through the memory chips by the read/write control logic. Parallel-to-serial converter output is clocked into the dropout compensator circuits where, when a dropout is indicated, the luminous data and inverted chrominance from two lines previous are inserted in the data stream. The time-base error data previously digitized modifies the reference 4Fsc input to produce a read 4Fsc signal. Video is routed through an additional path wherein chroma is extracted, amplified, and reinserted in the video. This signal is sent to the D/A converter in the Video Output PWA, accomplishing time-base correction. The analog output is routed through a low pass filter (equalizer), chroma level control circuit, and blanking adder. Burst and combined sync are all added to the video as the last stage before video output.

2-5 VIDEO INPUT PWA

The Video Input PWA provides the following functions:

- Selects, clamps, and amplifies off-tape video signal.
- Switches between input or TBC-processed video for video monitor output.
- Extracts sync from input video for processing in the Tape Clock PWA.
- Converts analog video input signal levels to 8-bit binary numbers.
- Develops a coherent relationship of chroma to luminance in heterodyne video operation.
- Decodes and encodes chroma data to simulate a color frame in slow-motion mode.

- Extracts off-tape burst and converts it to TTL levels which are sent to the Tape Clock PWA.
- Detects and indicates input video level and synchronization conditions (video high, video low, and burst present).

Discussion of the Video Input PWA will refer to Figure 2-3 and include details on the following circuitry:

Input video processing
Monitor video
Sync stripper video
Tape vertical deflection
Tape H-sync and video mute
Burst processing
A/D video processing
Color present
Tape VCO controls
Color processor
Dropout

2-6 Input Video Processing

Off-tape video selection, clamping, and amplification is done within the input video processing circuitry. The input video circuits are calibrated to provide 2-Vp-p output (sync tip to white color bar tip). After the tape video passes through a clamped buffer it is routed to a video switch where either INPUT VIDEO A or INPUT VIDEO B is selected for use within the TBC-6. The clamping circuit is set to maintain a back-porch level of 0V. The clamp is inhibited when there is no sync and is enabled by an output (input clamp) from the sync strip video circuits. When the clamp is inhibited (no sync), there is no output from input video processing circuits. The final stage of input video processing is a X2 amplifier. The amplification factor may be varied by the front panel VIDEO IN LEVEL adjustment. Sync stripper video from the X2 amplifier is routed to the sync strip video circuits for sync processing.

2-7 Monitor Video

Monitor video circuits select between the TBC input and TBC processed output. Video is routed to a MONITOR VIDEO select circuit. When in BYPASS, input video is sent through an amplifier to the MONITOR VIDEO OUT jack on the rear of the TBC-6. In NORM completely processed TBC video is available at the jack.

2-8 Sync Strip Video

The sync stripper video circuits extract sync (50% sync) that is used to develop signals to be processed in the Tape Clock PWA. The clamped video is amplified and passed through a chroma bandstop filter. The resulting video is buffered, amplified, and routed to a sync tip detect circuit (STDC). The STDC is comprised of a crude and a fine sync slicer and a sampler. The crude sync slicer utilizes a comparator to develop a sync TTL pulse (50% crude) that drives negative when the sync pulse

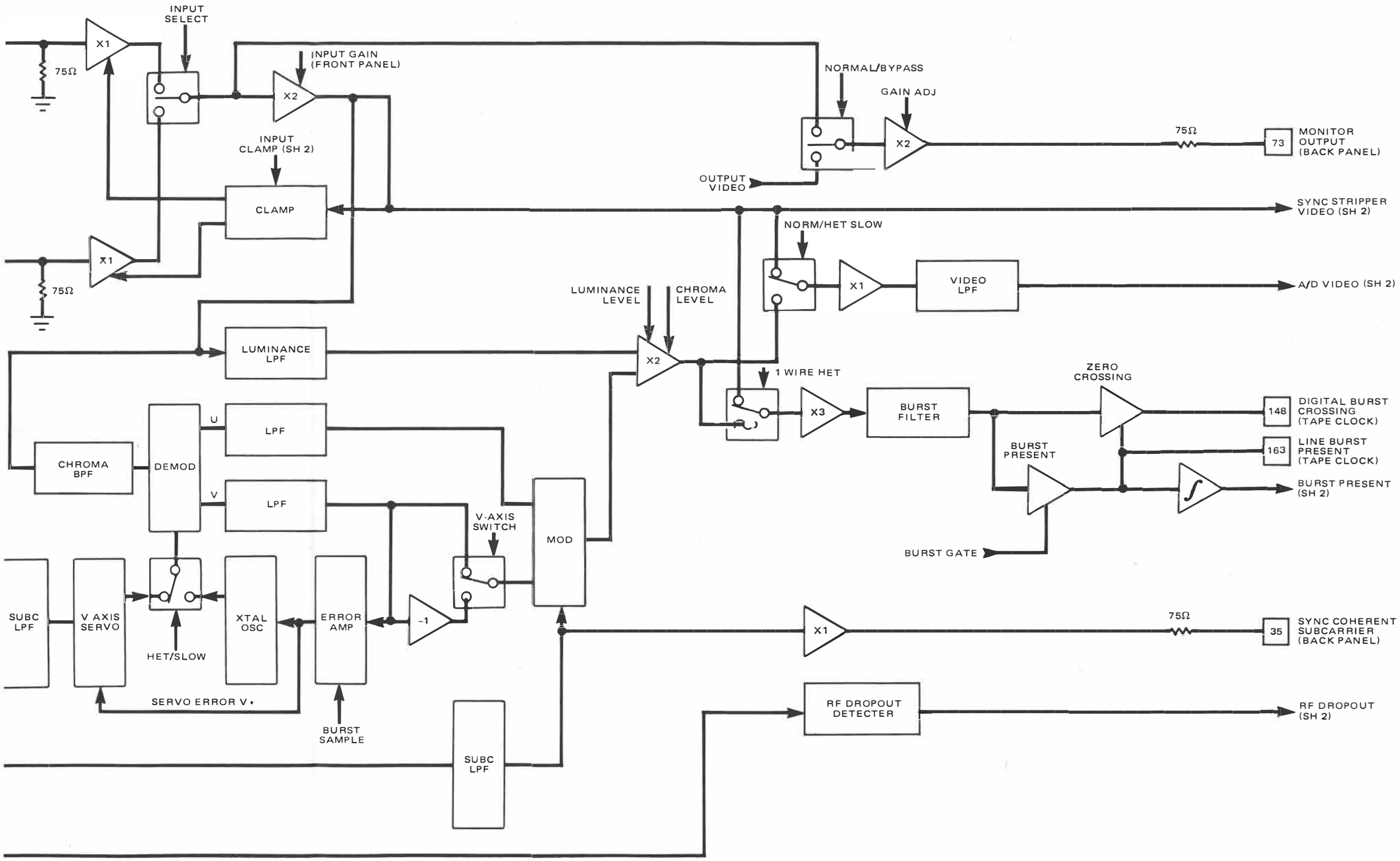
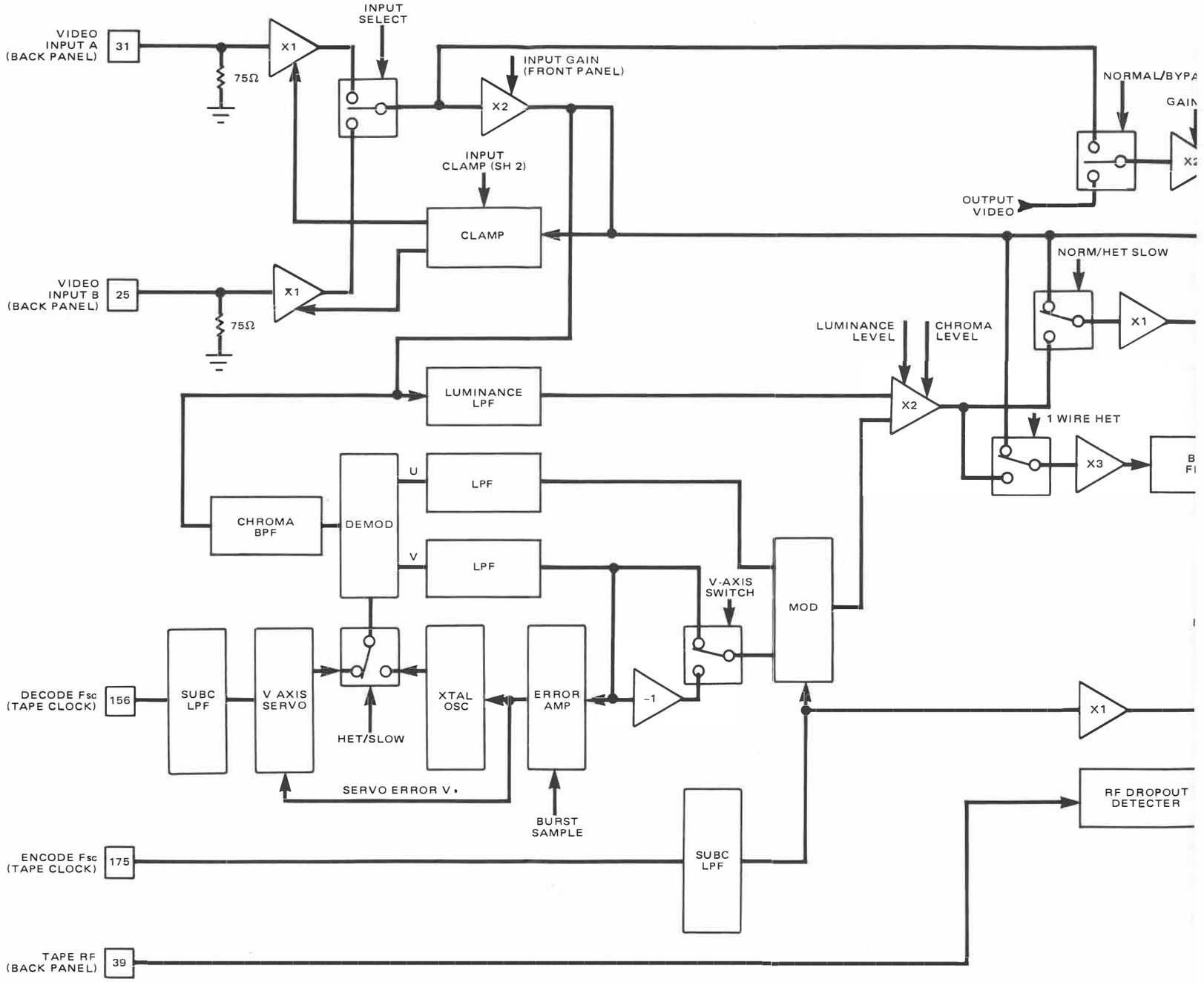


Figure 2-3.
Input PWA, Block Diagram
(Sheet 1 of 2)



Ampex 1809670-01

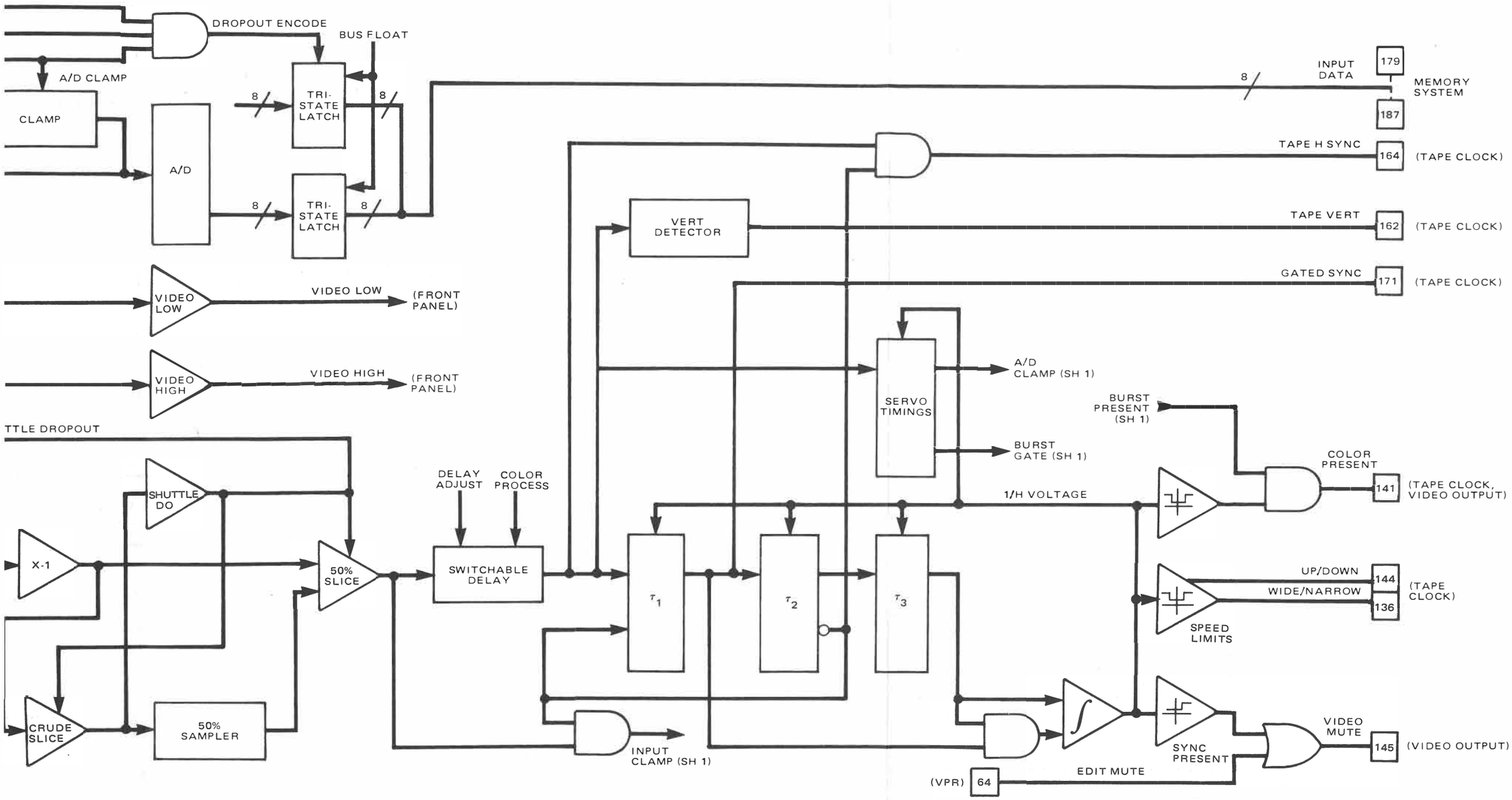
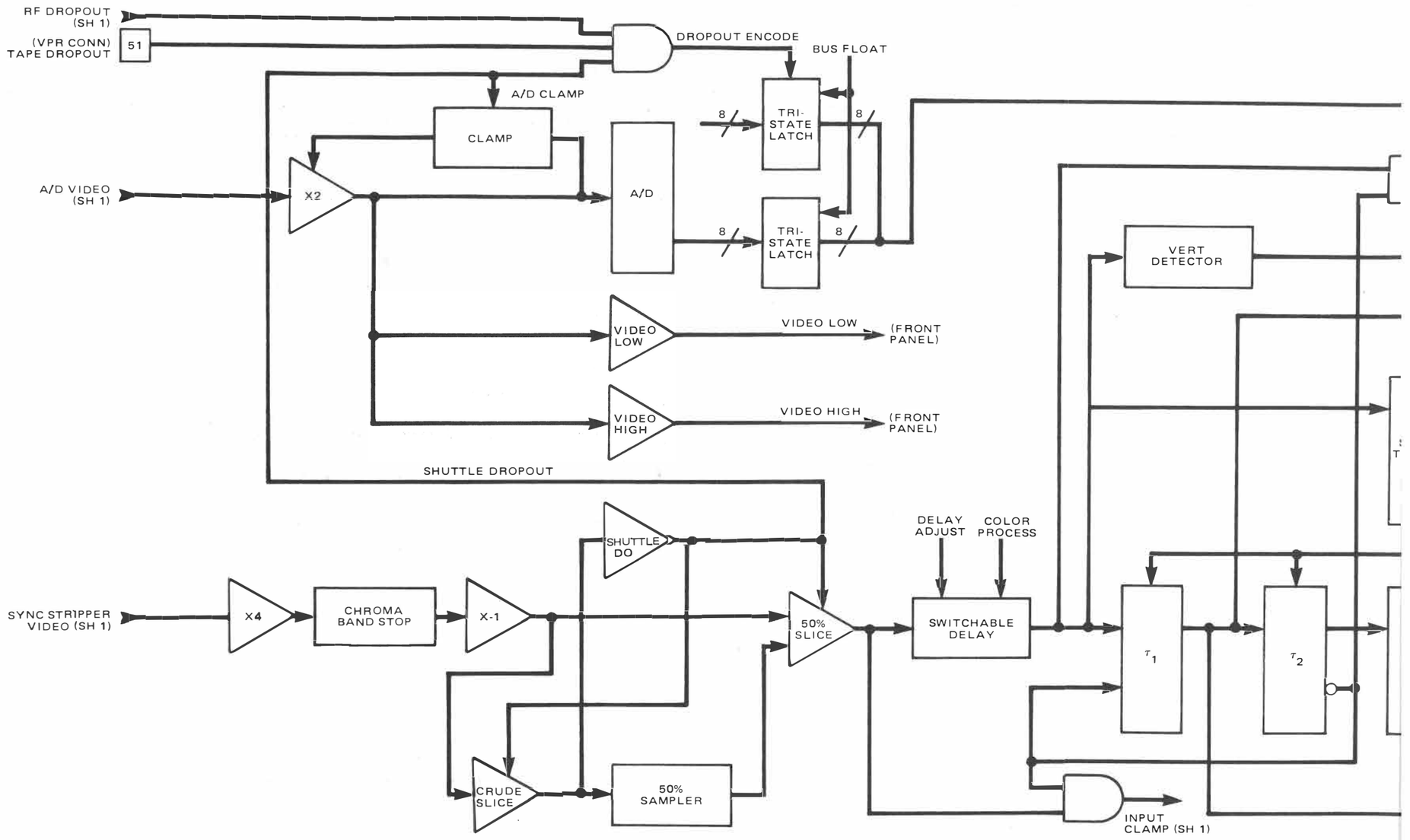


Figure 2-3.
Input PWA, Block Diagram
(Sheet 2 of 2)


RF DROPOUT (SH 1)
(VPR CONN) TAPE DROPOUT
51
DROPOUT ENCODE
BUS FLOAT
A/D CLAMP
CLAMP
8
TRI-STATE LATCH
8
A/D VIDEO (SH 1)
X2
A/D
8
TRI-STATE LATCH
8
VIDEO LOW
VIDEO LOW
(FRONT PANEL)
VIDEO HIGH
VIDEO HIGH
(FRONT PANEL)
SHUTTLE DROPOUT
VERT DETECTOR
SHUTTLE DO
DELAY ADJUST
COLOR PROCESS
SYNC STRIPPER VIDEO (SH 1)
X4
CHROMA BAND STOP
X-1
50% SLICE
SWITCHABLE DELAY
τ_1
τ_2
CRUDE SLICE
50% SAMPLER
INPUT CLAMP (SH 1)

crosses an estimated 50% point in a negative direction and drives positive when the sync reaches the 50% point going in a positive direction. The 50% crude pulse drives a sampler where sync tip and back porch level are extracted. By adding sync tip and back porch level and dividing by two an analog 50% sync voltage is obtained. By routing this analog sync through a comparator (fine sync slicer) using the input sync as the other comparator input, an exact 50% sync TTL signal is developed.

The STDC may be disabled by either a composite dropout signal or an HD SW/Vertical DO signal. The blacker-than-sync detector circuit utilizes the crude sliced sync to sense a noise spike on the video line. By feeding back a portion of the blacker-than-sync pulse (when noise is detected) the fine sync slicer is disabled and no 50% sync pulse is generated.

2-9 Tape Vertical Detection

The vertical detection circuits are all contained within the vertical detector block on the Video Input PWA block diagram. The broad pulse and equalizer pulse detection circuits, and equalizer pulse delay are all a part of the vertical detector. The 50% sync signal from the sync strip video circuits is processed to ensure that it is not a noise pulse and coupled into the broad pulse and equalizer pulse detection circuits as noise gate sync. The broad pulse detector output will normally be used to trigger the tape vertical pulse circuits within the Tape Clock PWA. However if no broad pulse is present (VPR-20 or certain heterodyne machines), the equalizer pulse detector output is used.

2-10 Tape H-Sync and Video Mute

The 50% sync signal from the sync strip video circuits is also used to generate four tape H-sync signals: clamp, burst gate, A/D clamp, and gated sync. Tape H is generated after the 50% sync pulse is processed to ensure that it is not a noise pulse and delayed to match the timing of burst. The H-gate control signal is a voltage that is inversely proportional to the period of sync. The H-gate control signal alerts the TBC when there is no video or which search VCO to use. Through use of a 6.5-, 55- and 1.5-µs delays, the various clamps and gates are generated. If the H-gate control signal is not of sufficient amplitude (no video), a video mute signal is generated and routed to the Memory System PWA. This inserts a blanking level into the video digital stream to the D/A converter.

2-11 Burst Processing

In the burst processing circuits, the off-tape burst is extracted and converted to a TTL level and sent to the Tape Clock PWA. The filtered video is amplified and routed through a burst filter and a burst detector. Output of the burst detector clocks a one-shot that generates a slow (changing) burst present signal. When composite dropout is active the one-shot is inhibited. The burst one-shot will also trigger a comparator that generates the digital burst signal.

2-12 A/D Video Processing

The A/D video processing circuits convert analog video input signal levels to 8-bit binary numbers. Analog video from the color processor or directly from the input

circuits, as selected by the input switch, goes to the A/D filter. The filter output goes to the A/D clamp which clamps the filtered video to the A/D reference level to establish a fixed, consistent level. The A/D converter samples the analog level using tape 4Fsc timing from the Tape Clock PWA.

The digital output is in an 8-bit binary coded form and is fed into a tri-state latch. When dropout is detected, the tri-state latch is disabled and a parallel latch is enabled and clocked (4Fsc). An FF binary code is placed on the data bus and sent to the memory circuits. When an overload is detected (FE or FF binary code), video follows the normal bus path and FE is routed to the memory circuits. Any lower binary code is an actual video representation but FF will trigger the detect, decode, and replacement switching dropout circuits in the Memory System PWA. The bus float signal disables both parallel latches while the tape clock inserts the line-by-line error code on the data bus.

2-13 Color Present

When the H-gate control is between 7.8V and 8.4V, the burst present signal establishes a color present signal.

2-14 VCO Controls

The H-gate control is extracted from the sync signal and routed through threshold circuits for processing in the Tape Clock PWA. Monitoring of the H-gate control provides a tape up/down signal and a tape wide/narrow signal based on tape speed. These signals are used to select the proper VCO. The up VCO is selected when the sync period is less than 51.7 µs and the down VCO when the sync period is more than 71.3 µs.

2-15 Color Processor

The color processor develops a coherent relationship of chroma-to-luminance in heterodyne video operation and decodes and encodes chroma to maintains color framing in slow-motion mode. Because of the one-quarter-cycle offset between the sync and subcarrier in the PAL I system (ignoring the 25-Hz offset), four distinct line types exist.

Off-tape video is processed in two primary color processor channels; a luminance channel and a chrominance channel. Normal video from the video input amplifier is supplied to a 2.5-MHz low-pass filter, which extracts luminance information, and a 3.58-MHz bandpass filter, which extracts chrominance information.

In slow-motion operation, a decode Fsc is defined from the input burst on the Tape Clock PWA and used to decode the input chrominance. The memory control defines which line type should be written into memory. It also determines if the V-component needs to be inverted in order to preserve the proper V-axis sequence. This information is used to create the encode Fsc signal on the Tape Clock PWA and to invert the V-axis component in the color processor when necessary. The encode Fsc signal is then used to reencode the U- and V-chrominance components into a new subcarrier. This subcarrier is then combined with the luminance information to create the color processed video which is then digitized in the A/D converter.

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In one-wire heterodyne operation, chrominance information is supplied to a demodulator. This demodulator also receives a stable 3.58-MHz carrier from a burst locked voltage-controlled crystal oscillator (VCXO). The burst oscillator gate is sampled by a switch and routed to an error amplifier in the burst locked oscillator.

During heterodyne operation, a video signal is received in which the chrominance component is not sync coherent with the luminance component. Before this signal can be time-base corrected, the sync coherence of the chrominance component must be established. To accomplish this, the chroma is extracted from the luminance component by a decode subcarrier which is phase-locked to the average vector of the off-tape swinging burst. The decode U- and V-signals are reencoded with a subcarrier which is sync coherent. Luminance is processed in a separate channel and delayed sufficiently to match the delay of the processed chroma. The two components are recombined, clamped and amplified to the correct level.

2-16 Composite Dropout

This signal is developed from either VPR dropout, rf dropout, or blacker-than-sync detector output. The composite dropout is stretched and routed directly to the A/D latching circuits.

2-17 TAPE CLOCK PWA

Figure 2-4 is a block diagram illustrating the functional relationship between circuits within the Tape Clock PWA. The Tape Clock PWA receives signals from the Video Input PWA and provides time-base error data and write timing for the Memory System PWA. The Tape Clock PWA also generates the tape 4Fsc signal used in the Video Input PWA and Memory System PWA.

The TBC-6 contains three VCO circuits, one normal VCO and two search VCOs. At normal play and slow-motion speeds, the normal VCO tracks incoming horizontal sync and provides a sync gate which prevents noise from triggering the horizontal sync circuits. In forward or reverse shuttle speeds, the search VCOs, which have a wider range and lower accuracy than the normal VCO, track incoming horizontal sync.

The Tape Clock PWA provides the following functions:

- Processes vertical and horizontal sync from the Video Input PWA and the VTR to provide tape-referenced timing for use throughout the TBC.
- Generates tape 4Fsc locked to a selected burst crossing during normal operation and locked to tape-H during forward or reverse shuttle, heterodyne or black and white operations.
- Generates encode Fsc and decode Fsc used in slow motion operation and with heterodyne video input signals by the color processor on the Video Input PWA.
- Generates write timing signals for use by the Memory System PWA.
- Measures line error information and converts it to two bytes which are sent to the Memory System PWA as the last two bytes of the data in a line of digital video.

The discussion of the Tape Clock PWA refers to Figure 2-5 and includes details on the following circuits :

Tape vertical processing
Tape horizontal processing
Normal VCO
Search VCO
Multiplexer output logic

2-18 Tape Vertical Processing

Within the tape vertical processing circuits (TVPC) the off-tape vertical sync is used to generate tape referenced vertical timing throughout the TBC. Inputs to the TVPC are the P/B vertical, slow motion, TTL dropout, head switch/vertical dropout, and sync head process from the VPR-6 interconnect cable, plus tape vertical from the Video Input PWA. In normal play, tape vertical or P/B vertical will be selected to preset a line counter that counts up to the next vertical interval to generate a window that brackets the vertical interval. This VCO phase comparator inhibit signal will disable the phase comparator during the vertical interval. The reset-qualify pulse enables the reset logic to rephase the normal counter. By resetting the normal counter with a tape-H timing pulse derived from tape burst, the normal VCO outputs are rephased at the beginning of the field without slewing the frequency of the 4Fsc oscillator.

2-19 Tape Horizontal Processing

The tape horizontal processing circuits (THPC) convert the off-tape horizontal sync into tape referenced horizontal timing, measure line error information for use in time-base error computation, and contain the logic required to operate the EDIT READY and the INVERT indicators. To determine the phase relationship between tape H-sync and tape burst, it is first necessary that the H-sync track a tape burst. Off tape H-sync is modulated by a 25-Hz ramp to generate burst coherent H which is processed to form a window around a selected burst crossing. In the event the burst crossing moves with respect to tape-H, a phase difference is measured. This difference is converted to a dc level by a ramp generator and then, through servo action, the burst crossing select window will follow variations in sync/burst timing.

EDIT READY lights when the burst-to-sync phase is within ±40° of a reference set by the CALIBRATE control. When CALIBRATE is positioned to detent, EBU standards are in effect for burst-to-sync phase positioning. When burst-sync phase deviates 135° or more from the reference set by CALIBRATE, a dump circuit discharges, the burst crossing selector flips 180°, and burst-to-sync is remeasured. The vertical inhibit signal input disableS the circuit during vertical interval.

Line-by-line error is measured by comparing the burst crossing to tape 4Fsc and producing a TTL pulse, the width of which reflects the error measurement of that particular line. The width of the pulse is converted to a ramp in the ramp generator. The output of the ramp generator is digitized and routed to a tri-state buffer and control circuit and on to the Memory System PWA. The tri-state buffer and control circuit is enabled by the vel comp write signal. The analog signal from the ramp generator is also used to generate the encode and decode Fsc clocks.

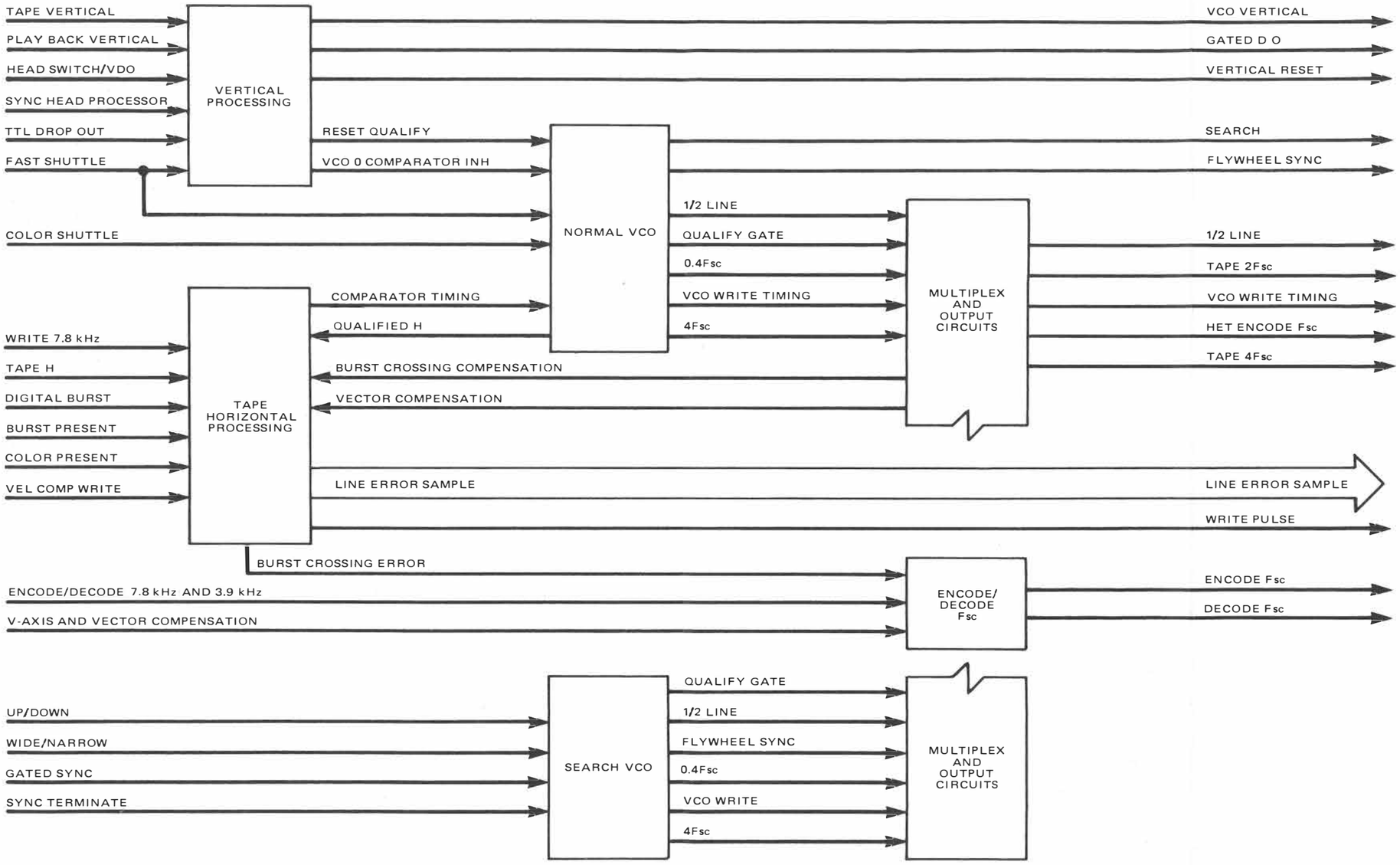

Figure 2-
Tape Clock PW
Simplified Block Diagra

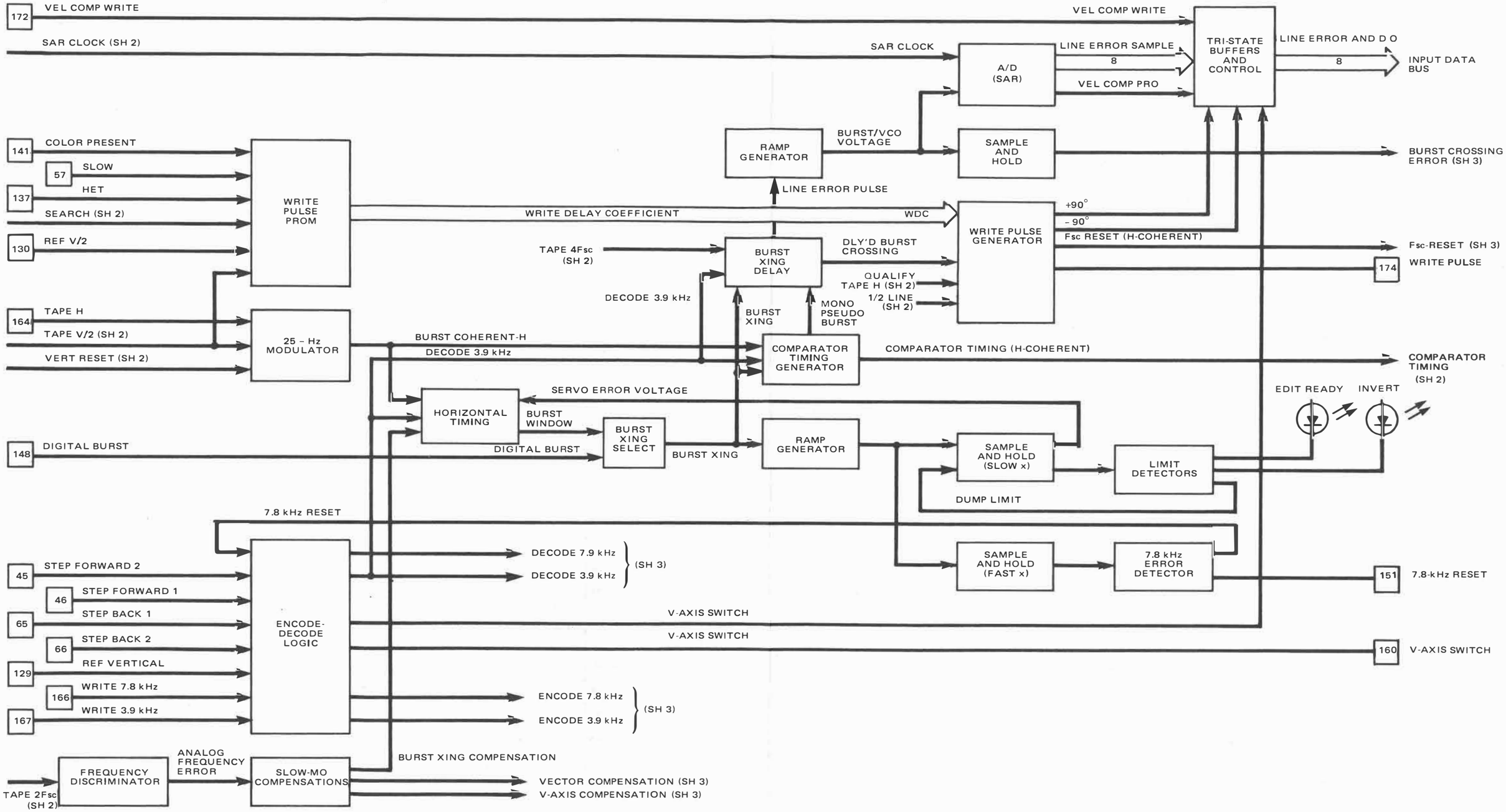

Figure 2-5.
Tape Clock PWA, Block Diagram
(Sheet 1 of 3)

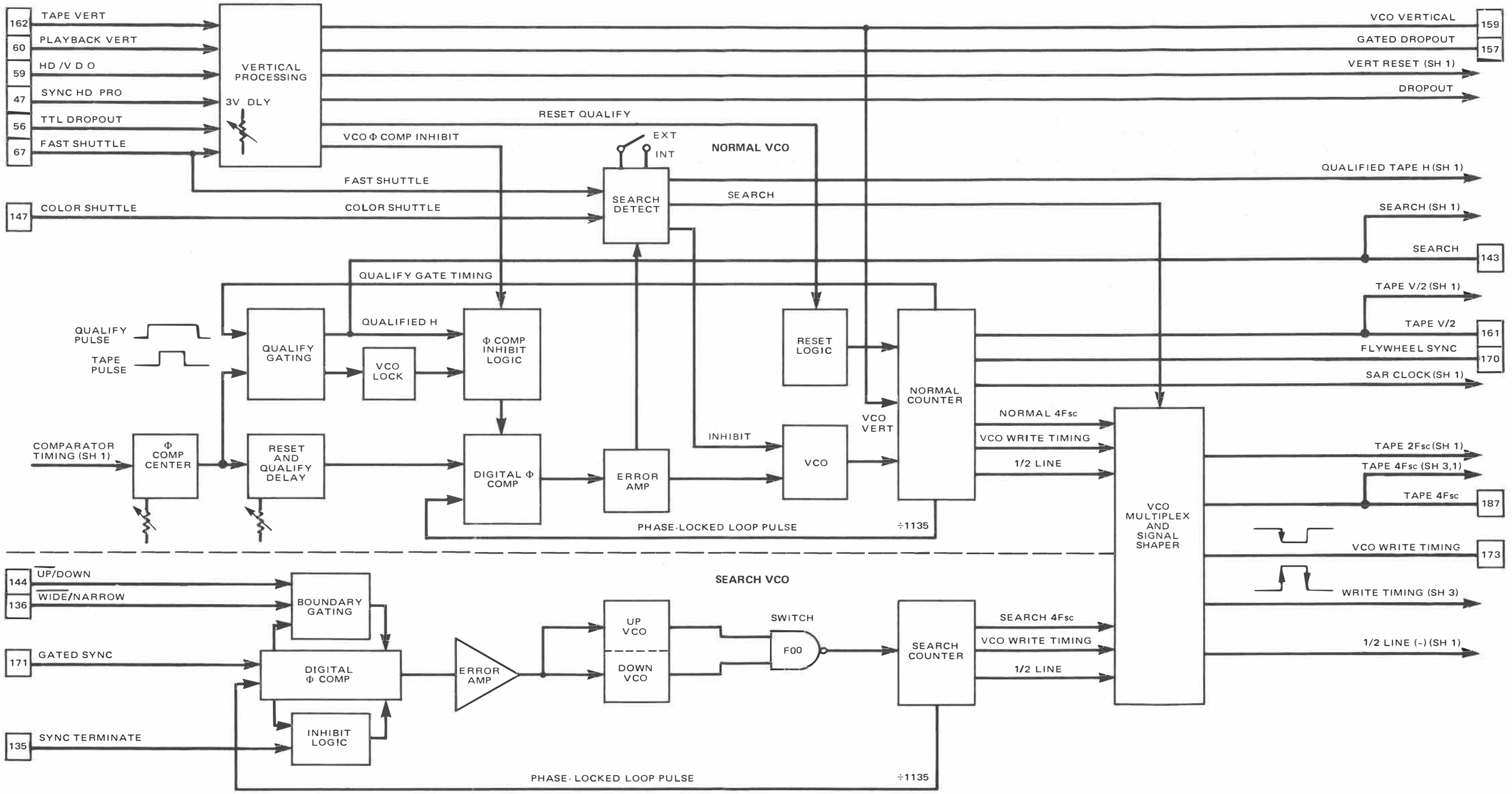

Figure 2
Tape Clock PWA, Block Diagr
(Sheet 2 o

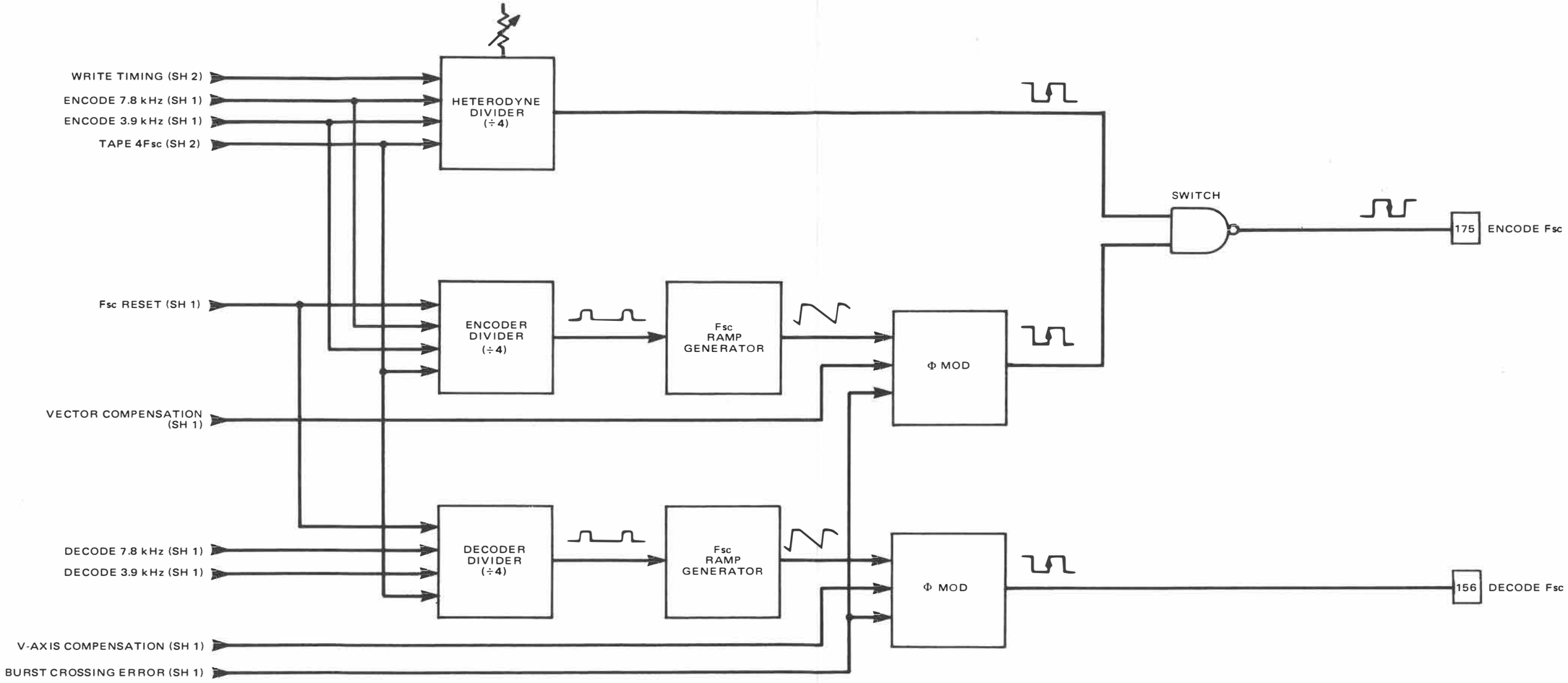

Figure 2-5.
Tape Clock PWA, Block Diagram
(Sheet 3 of 3)

2-20 Normal VCO

The normal VCO consists of a voltage-controlled oscillator, a digital phase comparator, and a normal counter. The normal VCO 4Fsc output clocks the divide-by-1135 normal counter. One output of the normal counter is an H-rate pulse, designated phase-lock loop pulse. This pulse is one input to the digital phase comparator (DPC). The other phase comparator input is a comparator timing pulse derived from tape burst. If the phase-locked loop pulse and the comparator timing pulse are in phase, the output of the DPC remains at a constant dc level. If there is a phase change, the voltage changes to vary the VCO frequency. The normal counter outputs are routed to the VCO multiplexer along with a search (VCO select) signal from the search detect circuit. The search detect circuit will continually monitor the error amplifier in the normal VCO circuit and when the normal VCO unlocks the search control circuit switches from the normal VCO to the search VCO. When the normal VCO relocks, the normal VCO is again used.

The internal/external switch, when in external, monitors the AST in the VPR-6 and thus keeps the normal VCO on the line in shuttle speeds as long as the AST is locked on. When the heterodyne switch is actuated, the internal/external switch defaults to internal. Other outputs from the normal counter are the tape V/2 and flywheel sync (sent to other PWAs) and the normal 4Fsc, VCO write timing, and half-line (sent to the VCO multiplexer and signal shaper).

2-21 Search VCO

The search VCO consists of two similar voltage-controlled oscillators. One oscillator is used in forward shuttle mode and one in reverse shuttle mode. Oscillator selection is controlled by VCO up/down and wide/narrow signals from frequency detector circuits on the Video Input PWA and the search signal within the Tape Clock PWA. Operation of the two oscillators is similar: the search 4Fsc output clocks a search counter. The resultant H-rate pulse is delayed and sent to one input of a phase comparator as the counter pulse. The other input to the phase comparator is gated sync from the Video Input PWA. If the selected oscillator output is not in phase with gated sync, a correction voltage is applied to the VCO and the outputs are brought back in phase.

The decode Fsc circuitry utilizes a 4Fsc signal to generate an Fsc that corresponds to the tape subcarrier. In the decode divider, the circuit is clocked by tape 4Fsc and the divider is preset by decode 7.8 kHz and 3.9 kHz during the Fsc reset cycle. Divider output is used to generate an Fsc ramp that is sent to the phase modulator. The signal that modulates this Fsc ramp is an error signal comprised of burst crossing error (line-by-line error) and V-axis compensation. The modulated Fsc signal assures that the decoding is done on axis throughout the slow motion range.

2-22 Multiplexer Circuits

In addition to selecting the appropriate VCO output, the multiplexer circuits generate VCO write timing signals for use in the Memory System PWA and write timing signals to be used in the encode/decode circuits.

2-23 Encode/Decode Fsc

The encode and decode circuits utilize dividers (counters), ramp generators, and phase modulators to generate the encode and decode Fsc signals used in the color circuitry and an encode Fsc signal used during heterodyne operation.

During heterodyne the decode Fsc is generated by a burst lock oscillator on the Video Input PWA. The heterodyne portion of the encode Fsc circuit consists of a divider clocked by tape 4Fsc and preset by encode 7.8 kHz and 3.9 kHz during the write timing pulse reset cycle. Output from this circuit is routed to a switching network that selects either heterodyne divider output or the encode phase modulator output.

Encode and decode Fsc signals are generated on the tape during slow motion. The encode Fsc circuitry utilizes 4Fsc to generate an Fsc that corresponds to the phase of subcarrier required by the memory load. In the encode divider the circuit is again clocked by tape 4Fsc and the divider is preset by encode 7.8 kHz and 3.9 kHz during Fsc reset cycle. Divider output is used to generate an Fsc ramp that is sent to the phase modulator. The signal that modulates this Fsc ramp is an error signal comprised of burst crossing error (line-by-line error) and vector compensation. The modulated Fsc signal assures that the proper chroma phase is maintained throughout the slow motion range.

2-24 MEMORY SYSTEM PWA

Figure 2-6 is a simplified block diagram of the Memory System PWA illustrating the relationship between the different functional blocks within the PWA.

The Memory System PWA receives 8-bit data (input data) representing instantaneous video level, sampled at a tape 4Fsc rate, in byte-serial fashion which is routed into the write-in buffer in the memory circuits video path. A complete read/write cycle takes one superword to complete and consists of a write cycle A, a write cycle B, and a read cycle. Input timing for the write-in buffer is based on tape 4Fsc while all other timing within the memory is derived from reference 4Fsc. WIA and WIB, both early (E) and late (L), supply addresses for the input data. Sixteen bytes are combined in one superword and written into main memory in their respective locations during write cycle A. During write cycle B, the operation is determined by the selected mode.

During write cycle B in normal speed, E-E, slow motion, and reverse shuttle, the same superword is loaded into a memory location four video lines ahead.

During slow motion, normal speed, and E-E, input data rate is very close to output data rate. Therefore the write-in buffer has sufficient capability to handle the rate differential. This operation allows for a gentle overload.

During reverse shuttle, the input data rate is considerably less than the output rate and consequently superwords are not always available for input to the main memory. It is also often necessary to repeat video lines in order to properly center the video image. This will ensure that the read function always has a valid line available to read out to the memory.

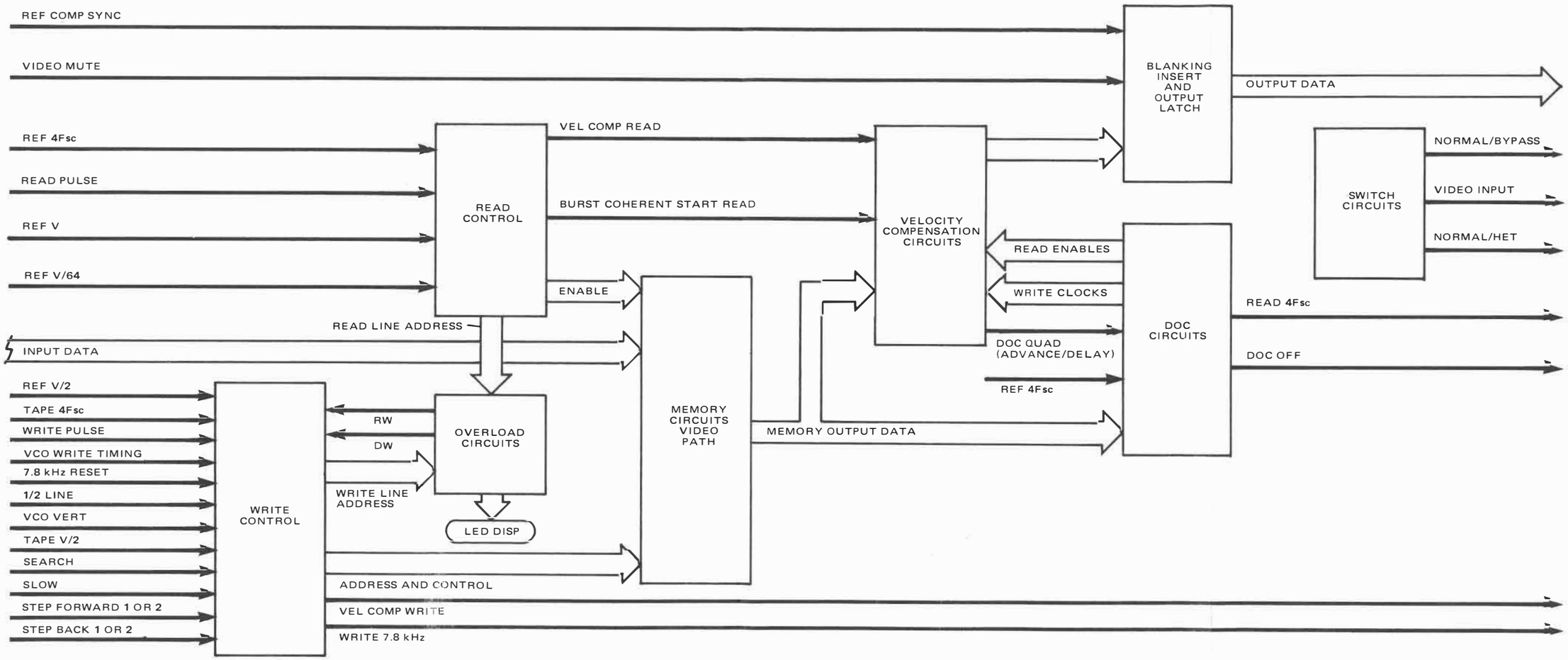

Figure 2
Memory System PW
Simplified Block Diagr

During forward shuttle, input data rate is considerably faster than output data rate. It is often necessary to write two superwords during one read/write superword cycle. The dual-load function makes this possible by allowing an input superword to be loaded into its respective location during write B as well as write A. The dual-load function is automatically entered whenever the write-in buffer is full.

In addition, it is often necessary to delete video lines in order to properly center the video image. This is done by decrementing the write line counter by four.

Output data from the memory circuits' video path consists of 8-bit data which is processed by DOC. When the DOC detects a video dropout, the dropout is replaced with the corresponding word from the line two lines previous. This 8-bit data is also routed to the velocity compensation logic which contains the time-base error profile generator. Reconstruction of the line-by-line error signal is performed in the time-base error profile generator. The next line-burst error and the present line-burst error are subtracted. This difference is used to form a first order approximation of the error difference (time-base error signal). This linear interpolation develops a time-base error signal that represents both line-by-line error and velocity error. This time-base error signal is used to produce a read 4Fsc signal from a REF FSC signal.

Finally, the 8-bit data goes to the blanking insert and output latch, which supplies data (time-base corrected) to the Video Output PWA. The error-corrected READ 4FSC clock is also sent to the Video Output PWA where time-base error correction is performed in the D/A converter.

The Memory System PWA provides the following functions:

- Stores 32 lines of digital video information in random-access read/write memory.
- Detects dropouts and replaces missing information.
- Compensates for line-by-line and velocity error.
- Presets Video Output PWA D/A converter circuit to binary equivalent of blanking level during blanking interval.

A discussion of the Memory System PWA refers to Figure 2-7 and consists of details on the following circuits:

Memory input video path
Read control logic
Write control logic
Overload control
Dropout compensation
Velocity compensation
Output latches

2-25 Memory Input Video Path

The memory input video path consists of the write-in buffer, the main memory, and the parallel-to-serial converter. The data rate seen at the input to the main

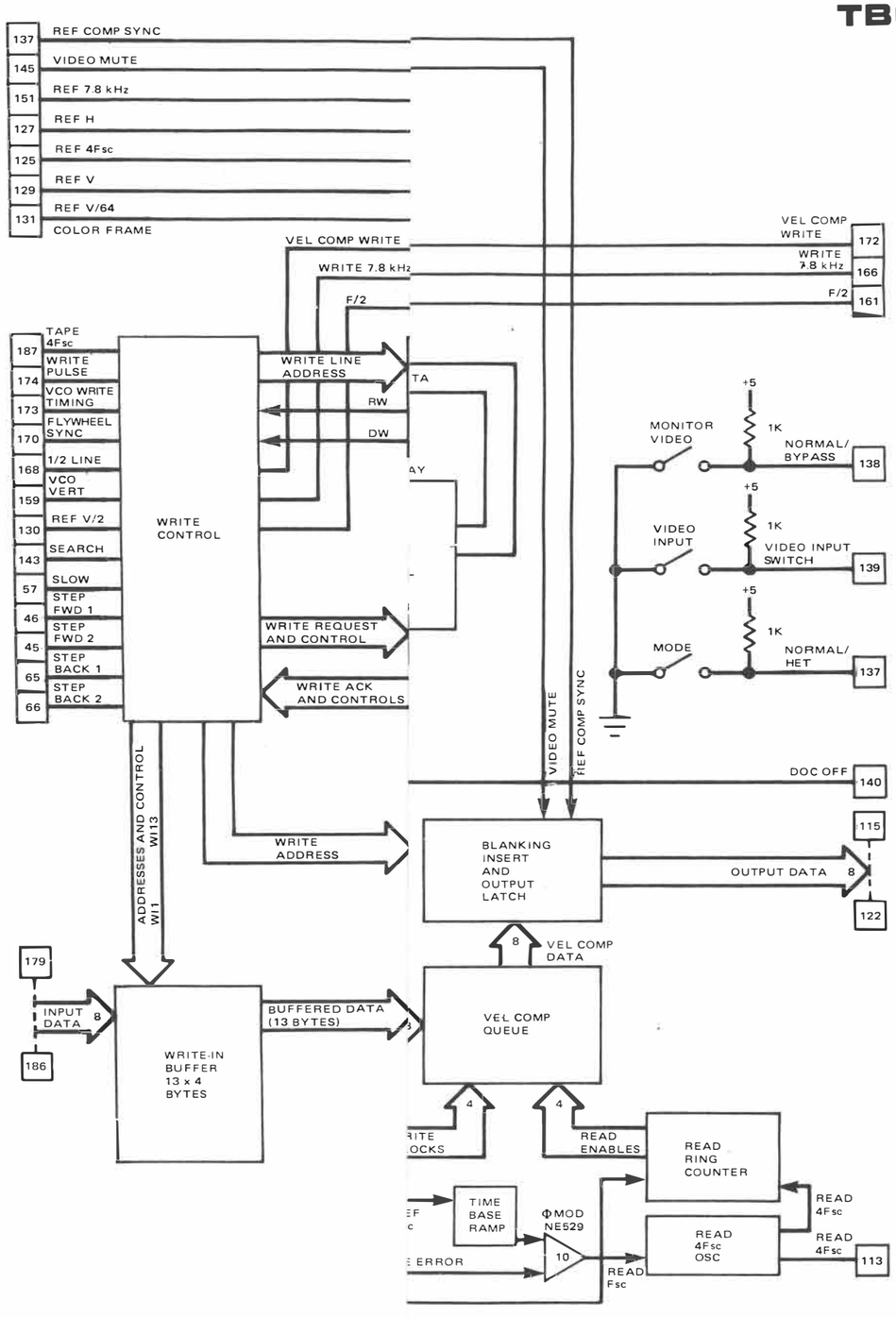

Figure 2-7.
Memory System PWA, Block Diagram

memory could range all the way from reverse to forward shuttle. The data is clocked into the write-in buffer at a tape 4Fsc rate and read out of the write-in buffer with respect to reference 4Fsc rate. To accommodate the timing difference, the write-in buffer has the ability to hold up to four superwords and to provide the serial-input function. The TBC-6 uses an array of byte-wide registers to buffer the data from the A/D Converter into superwords, each of which are 16 bytes long. Hence the entire matrix provides temporary storage for up to four superwords (one superword = 16 bytes) maximum.

2-26 Write-in Buffer

This circuit provides temporary storage of words and groups them into blocks of 16 bytes, (superwords). The buffer device pairs provide independent, asynchronous input/output transfer functions. Writing entails two address bits (WIA/WIB at the device) and a write enable. Reading entails two address bits (WOA/WOB at the device) and a read enable.

The read enable signals are labelled REA for the first eight pairs and REB for the remaining eight pairs. (Although these signals occur at the same time, they are derived from different drivers and thus have different labels). The two read address bits are labeled WOA and WOB.

2-27 Main Memory

The main memory is an array of random access memory (RAM) devices which can be written into and read out of memory randomly on separate read and write cycles. Superwords are accumulated in the write-in buffer and transferred to main memory. Main memory provides storage of 32 lines of video data with each line comprising 64 superwords.

Main memory involves a nominal 8-line delay of the data before it is read out of the RAM devices. The read timing, derived from the station reference (from Video Output PWA), clocks the data which is read out in parallel as superwords.

2-28 Parallel-to-Serial Converter

Superwords go to the parallel-to-serial converter, which converts them back into serial (byte-wise) words. The serial words are routed to the velocity compensation and DOC circuits. The parallel-to-serial converter is clocked by referenced 4Fsc.

2-29 Write Control Logic

The write process logic monitors write timing to determine if the write-in buffer is full, or if there is a superword available in the write-in buffer, and provides appropriate feedback to the write control logic.

In VPR-6 still-frame operation, the internal automatic scan tracking (AST*) circuits move the video reproduce head from track to track as required. Step forward and step back outputs from the VPR-6 are used to shift write addresses in the TBC-6 as required to follow the AST circuits.

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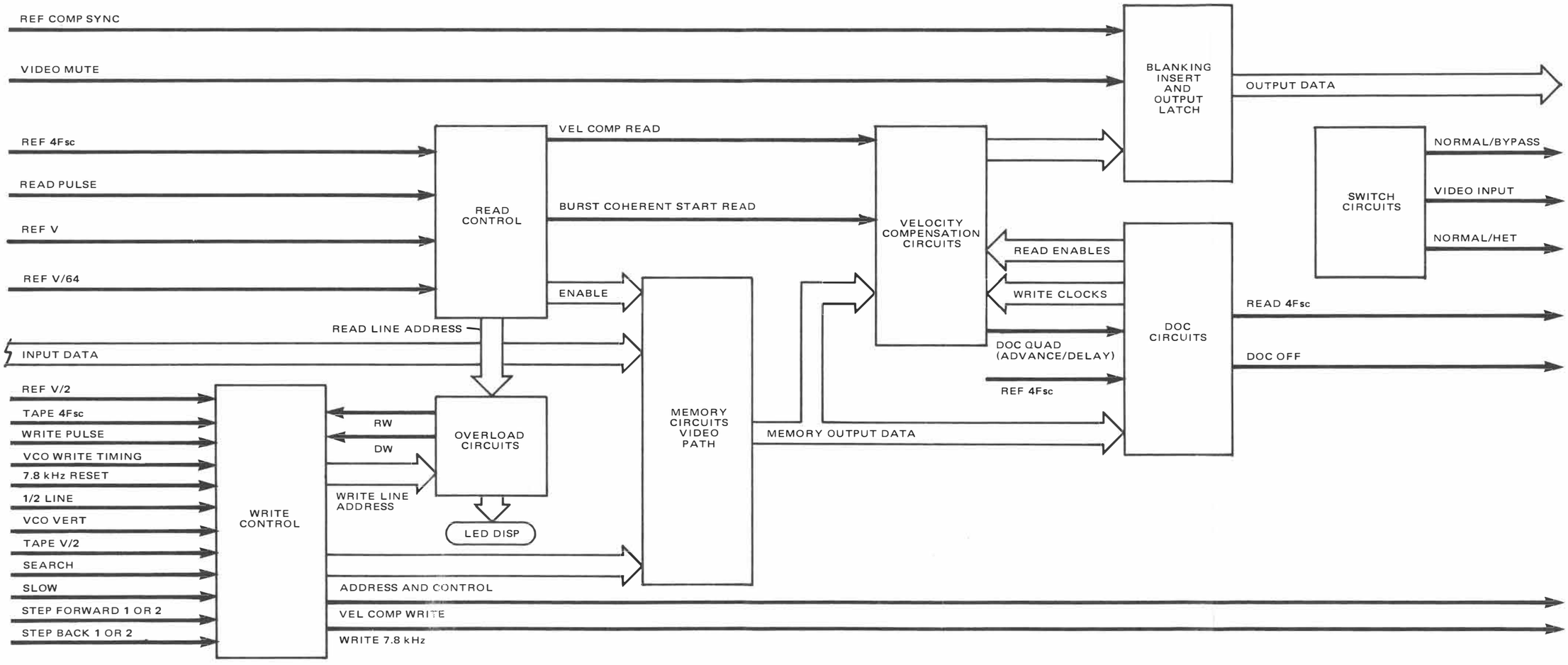

Figure 2-
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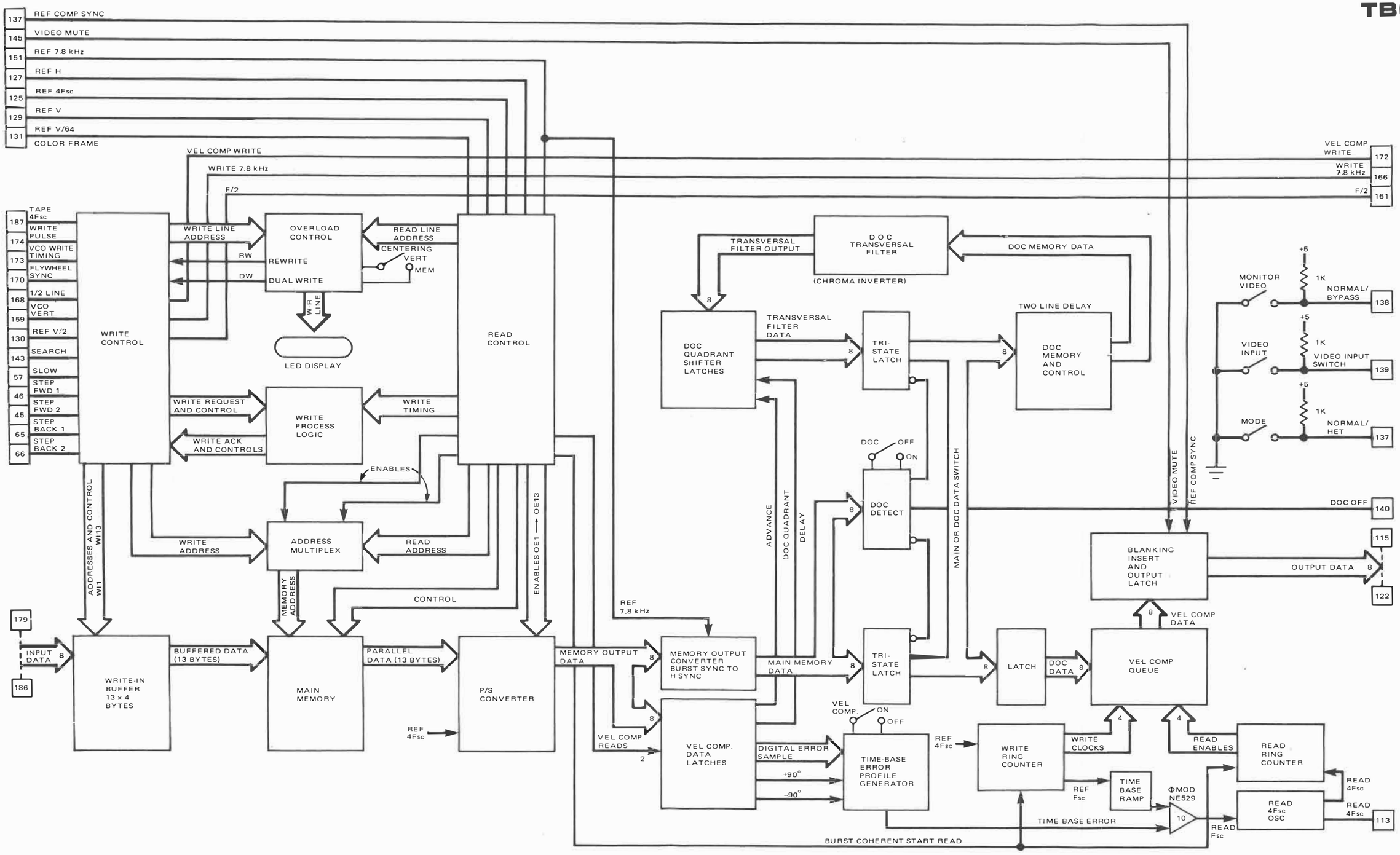

Figure 2
Memory System PWA, Block Diagr

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*Trademark, Ampex Corporation

2-30 Read Control Logic

Data is read from memory using timing derived from reference 4Fsc. Reference vertical presets a read line address counter which divides reference horizontal by 16. Reference 4Fsc drives a 16-bit shift register which is preset by reference horizontal and generates output enable signals OE1 through OE16. The read superword address counter generates read addresses A0 through A5, which correspond with the 64 superwords per line.

2-31 Overload Control

The overload control senses the line being written into memory and the line being read out of memory to determine if an overload is about to occur in either direction. The LED display indicates the difference between the write and read address.

2-32 Output Latches

Each of the 16 output latches is 8-bits wide and is enabled by a signal called OE1-OE16. These signals occur in 4Fsc increments, syncronous with the subcarrier of the station reference video signal. Parallel-to-serial conversion is also accomplished in the output latches. Each latch is clocked by a signal called READ which loads data from the memory at the appropriate time.

2-33 Dropout Compensation

Dropout detector circuits on the Video Input PWA encode hexadecimal FF in place of normal video data for the duration of a dropout. This data is transferred to memory, and detected by a dropout compensator (DOC). The DOC replaces missing video data with valid data from a corresponding portion of a line two lines previously recorded.

In the absence of a dropout, 8-bit data flows to the Memory System PWA output circuits. Data is also stored in a two-line read/write memory. Data read out of memory is selected in blocks of 8 bits and then processed by a digital filter circuit. This circuit inverts chroma data for use during a dropout. When the FF detector encounters a byte containing FF hexadecimal, processed dropout data from the two-line memory then flows to the PWA output circuits. In addition the same video data is recirculated through the dropout circuits in the event the next line also has a dropout.

2-34 Velocity Compensation

The velocity compensator circuits consist of a vel comp data latch, a time-base profile generator, a phase modulator, read 4Fsc oscillator, and a vel comp queue. The vel comp read signal turns on the vel comp data latches when bytes 14 (line-by-line error data) and 15 (90° phase shift error) of superword 64 are being clocked through the P/S converter The 90° phase-shift error is sent to the time-base error profile generator and the DOC circuits.

The time-base error profile generator takes digital time-base error data and develops a first order approximation of the time-base error.

The output is applied to a phase modulator which changes incoming reference 4Fsc phase to compensate for time-base error. Phase-modulated reference Fsc drives one input of a phase comparator. The other phase comparator input is the divided-down read 4Fsc output of VCO, which is also at subcarrier frequency. If the two-phase comparator inputs remain in phase, the output remains constant. If their relative phase changes, a correction voltage is applied causing the VCO's output to change in the direction of phase stability. In this manner, read 4Fsc is developed from reference 4Fsc.

The vel comp queue is used to compensate for phase changes between the reference and read 4Fsc signals. The write ring counter supplies the write clocks to the vel comp queue while the read counter supplies the read enables. Both ring counters utilize a burst coherent start read signal from the read control circuits to initialize the vel comp queue at the beginning of the line. The read 4Fsc output of the Memory System PWA is sent to the Video Output PWA, where the output is used as a clock for D/A conversion circuits.

2-35 VIDEO OUTPUT PWA

The Video Output PWA provides the following functions:

- Converts serial 8-bit data from the Memory System PWA to an analog video signal.
- Compensates analog video for D/A conversion frequency response and clamps video to reference black level.
- Adds sync, burst, and reference timing to time-base-corrected video.
- Provides VIDEO OUT 1 and VIDEO OUT 2 outputs from the TBC-6 and a processed TBC video signal to the to the input PWA
- Provides advanced reference sync to VTRs which do not have the capability to generate advanced sync internally.
- Receives reference video input and extracts synchronizing signals such as vertical, horizontal, blanking, subcarrier, and burst.
- Chroma phase, chroma, video, and black level settings.

It is on the Video Output PWA (sync generator) that a single oscillator is used to synthesize both reference subcarrier and reference sync signals. This operation is accomplished in three steps.

- First, phase-lock a reference 4Fsc oscillator to reference burst to establish a 4Fsc clock signal whose frequency represents the reference burst frequency. Because of the 25-Hz offset between sync and subcarrier frequencies in the PAL I system, the 4Fsc clock signal must be shifted down by 100 Hz before it can be used to generate composite sync signals.
- The second step thus involves the synthesis of an H-4Fsc signal (1135H) from the reference 4Fsc clock which is used to generate all of the reference H-related signals used on the Video Output PWA.
- The third step is a phase alignment between the reference Fsc and the output sync.

The discussion of the output video PWA refers to Figure 2-8 and includes details on reference sync and timing generation and video processing.

2-36 Reference Sync and Timing

In the reference sync and timing circuits, the reference 4Fsc oscillator is phase-locked to burst. The reference and burst detector generates a burst-present signal operates a mono/color switch. Burst from the band pass filter is routed to a phase comparator (enabled during the burst window) through the mono color switch. The phase comparator senses the relationship between a lock Fsc signal and reference burst. The lock Fsc has the burst swing, having been generated from 7.8 kHz. If the modulation on the lock Fsc is out of phase from the burst swing, the error amplifier sends a flip 7.8-kHz signal to the reference 7.8-kHz detector and the lock Fsc signal swing is shifted 180° to match the reference burst input.

In the PAL I system, a 25-Hz offset exists between sync and subcarrier frequencies so the 4Fsc clock signal must be shifted down by 100 Hz before it can be used to generate composite sync signals. Subtraction of 100 Hz from the 4Fsc oscillator output is accomplished in the phase delay, sin-cos generator, and modulator circuits. The reference oscillator 4Fsc output is sent to a phase delay circuit that generates two 4Fsc signals, one advanced by 45° and one delayed by 45°. The sin-cos generator utilizes the line counter output to generate two 100 Hz signals, 90° out of phase. Utilizing the four previously mentioned inputs the modulator produces a sine wave (4Fsc-100 Hz). The modulator output is routed to a slicer, creating H-4Fsc that is routed to an along-line counter (ALC) and a H-4Fsc divider.

2-37 Sync Generator

The sync generator develops and positions the various sync signals on the horizontal lines utilizing an H-4Fsc output from the modulator within the output video PWA. The entire process consists of identifying the 625 lines that make up the frame and generating a signal that corresponds to each particular line. A line type prom then encodes the line number into one of 11 line types. As this action is taking place pixel positions along each line are counted. The pixel positions are then divided into 12 segments (see Table 2-1) relating to the unique states of all the signals to be generated during the horizontal line duration. Having identified the segments on a given line type, sync signals can then be generated. The sync generator consists of a line counter, an ALC, a line PROM, a line type PROM, an advance sync PROM, and a normal sync PROM.

The line counter is clocked by the reference H signal while the V/2 signal ensures that the count will start at the first line of the frame. The zero offset will delay the start of the line count by eight lines while the sync retard delays the start of the line count by one-third of a field. The heterodyne input will disable any VPR phase change inputs during heterodyne operation.

The line counter identifies the line number for the line type PROM. The line counter generates a signal (A0—A11) 0—624 (line count) every line. The line type PROM decodes the line count from the line counter output and encodes this data into two, 4-bit data words (normal line type and advanced line type). This data is

routed to the normal and advanced sync PROMS and represents the type of line at that particular position in the frame.

The ALC is clocked by the H 4Fsc signal and counts the number of pixels (0—1134) along the line. This information is converted to addresses (along-line address) and routed to a line (segment) PROM. The line PROM decodes the along the line addresses and reencodes them to line segment addresses for use in the advance and normal sync PROMs. The bit 2 and 3 inputs to the ALC lock the counter up to a particular place along the line in respect to reference-H.

The advanced sync PROM and the normal sync PROM decode the two four bit data words (one from the line type PROM and one from the line PROM) into the actual sync signals needed at that time.

The H-4Fsc divider is preset by reference Fsc and 2Fsc at the time determined by sync V/2. This establishes H-Fsc and H-2Fsc signals which have a known phase relationship to reference Fsc and 2Fsc at the beginning of each frame.

2-38 Sync/Burst H-Calibrate Circuit

The reference sync/burst H calibrate circuits execute the last step in synthesizing the reference subcarrier and the reference sync signals from a single oscillator. The synthesized black burst signal is phased up to the input reference within this circuit. The sync/burst calibrate circuit constantly monitors the error between reference-H and output-H and generates the signals (BIT 2 and BIT 3) required to phase adjust the output sync to return the system to a lock mode.

2-39 System Timing

The operator can adjust system timing with respect to reference using three levels of control. The H-range control (coarse) adjusts the system timing in steps of subcarrier cycles. The H-phase control (medium) adjusts the system timing in steps of 90° of subcarrier, and the subcarrier phase control (fine) adjusts the system timing within 90°. The H-range and H-phase controls feed an H-phase PROM that converts these inputs to values usable by the H-delay counter. The H-delay counter is enabled by the advance H-pulse and clocked by H-4Fsc, generating the delay H-pulse. Advance-H is at a specific location in the line, and by changing the time delay between advance-H and delay-H the position of output-H is corrected. The circuitry ensures that delay-H follows all movements of reference-H. This determines the location of output sync with respect to reference. In addition the H-delay counter uses the H phase control outputs to generate the lock Fsc Q_0 and lock Fsc Q_1 signals. The lock Fsc Q signals select the particular phased Fsc signal required by the lock Fsc.

2-40 Reference Divider

The reference divider has inputs of 4Fsc, lock Fsc $Q_{1,2}$, and 7.8 kHz and from them generates reference 2Fsc, reference Fsc, four phases of Fsc, burst Fsc and lock Fsc. In addition, this circuit applies the swing to burst Fsc and lock Fsc and also select the proper Fsc phase to be used by lock Fsc.

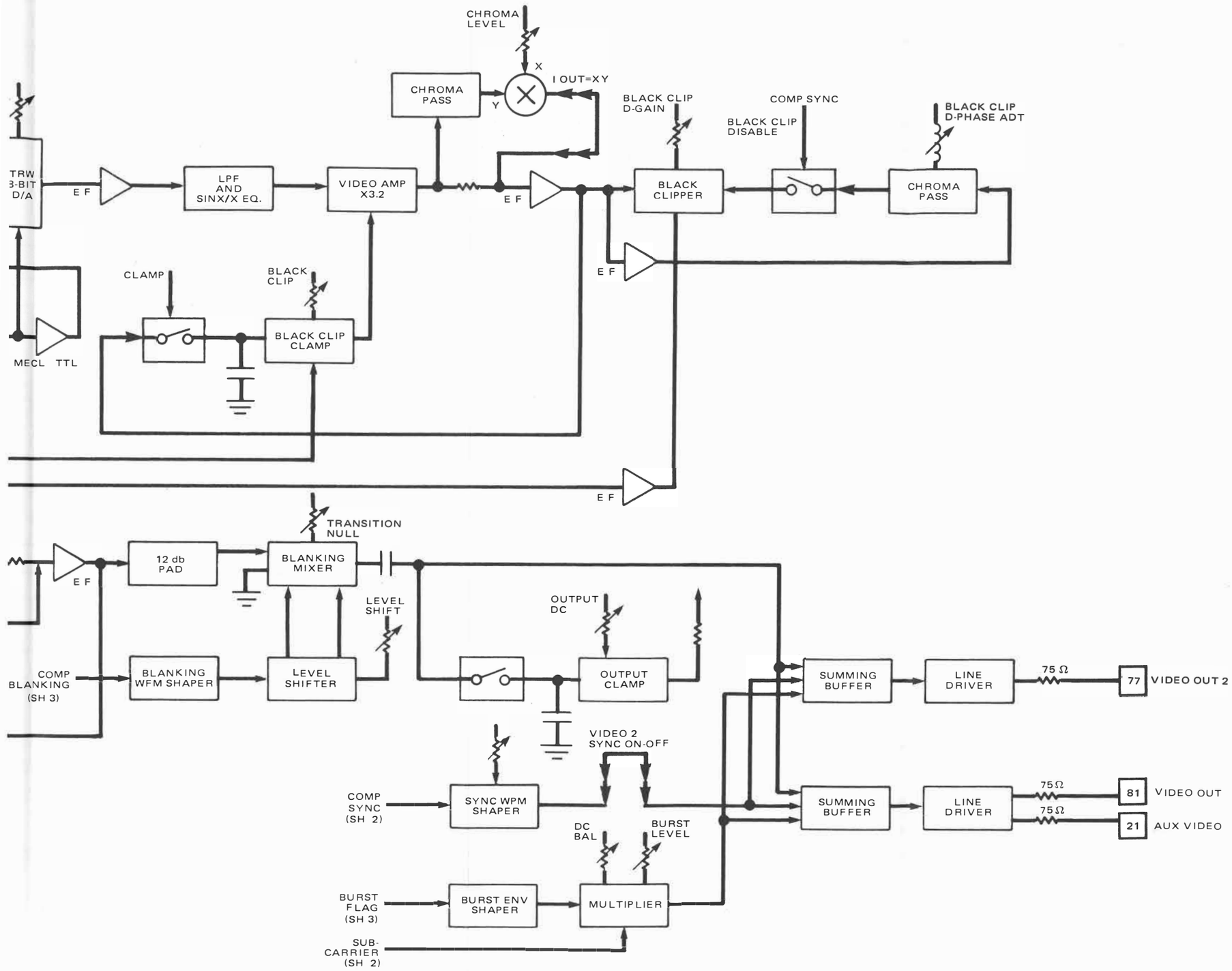
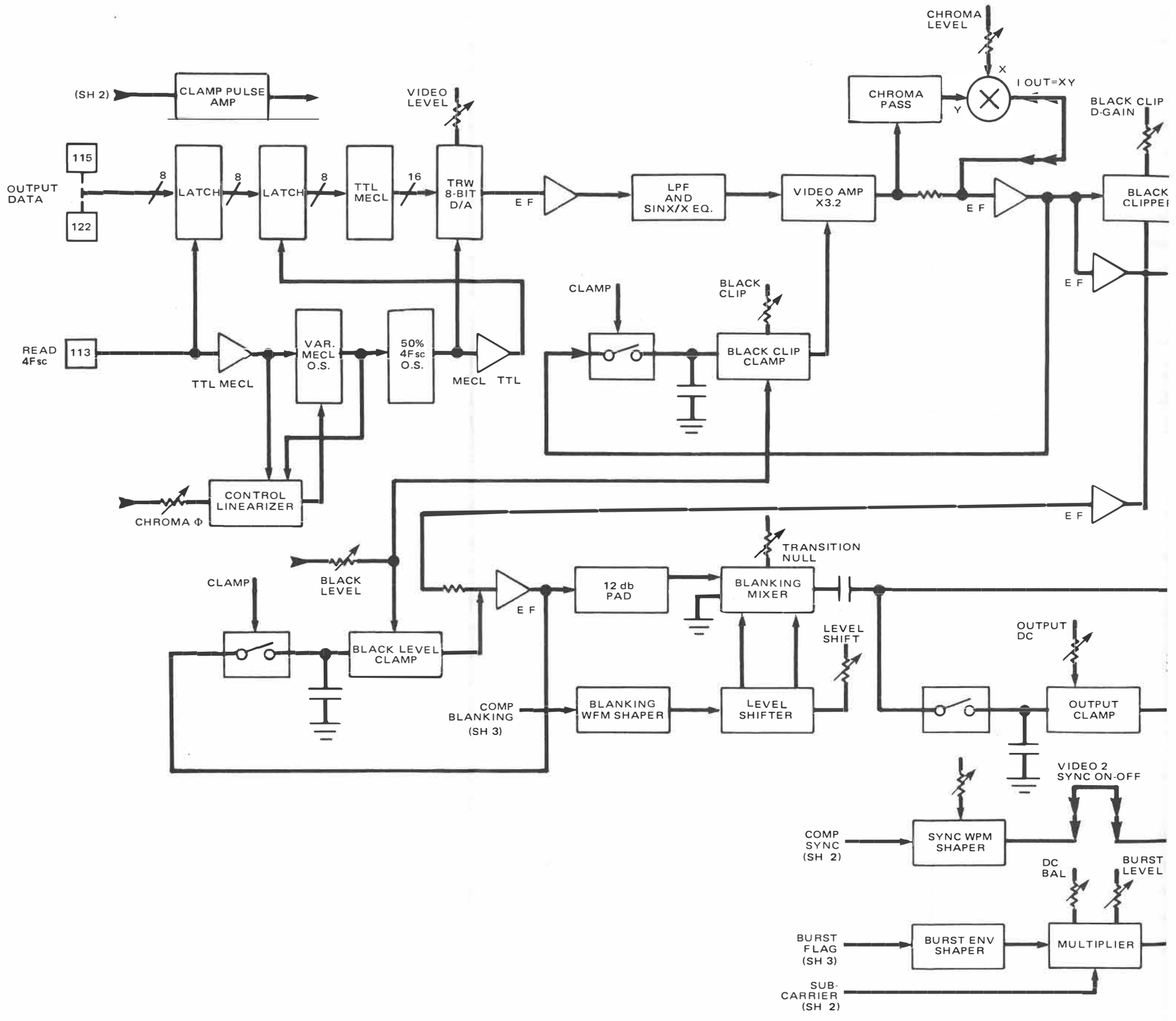


Figure 2-8.
Video Output PWA,
Simplified Block Diagram
(Sheet 1 of 3)


CHROMA LEVEL
X
I OUT=XY
Y
CHROMA PASS
(SH 2)
CLAMP PULSE AMP
VIDEO LEVEL
BLACK CLIP D-GAIN
115
OUTPUT DATA
122
8
LATCH
8
LATCH
8
TTL MECL
16
TRW 8-BIT D/A
E F
LPF AND SINX/X EQ.
VIDEO AMP X3.2
E F
E F
CLAMP
BLACK CLIP
READ 4Fsc
113
TTL MECL
VAR. MECL O.S.
50% 4Fsc O.S.
MECL TTL
BLACK CLIP CLAMP
CONTROL LINEARIZER
CHROMA Φ
E F
TRANSITION NULL
CLAMP
BLACK LEVEL
12 db PAD
BLANKING MIXER
E F
LEVEL SHIFT
OUTPUT DC
BLACK LEVEL CLAMP
COMP BLANKING (SH 3)
BLANKING WFM SHAPER
LEVEL SHIFTER
OUTPUT CLAMP
VIDEO 2 SYNC ON-OFF
COMP SYNC (SH 2)
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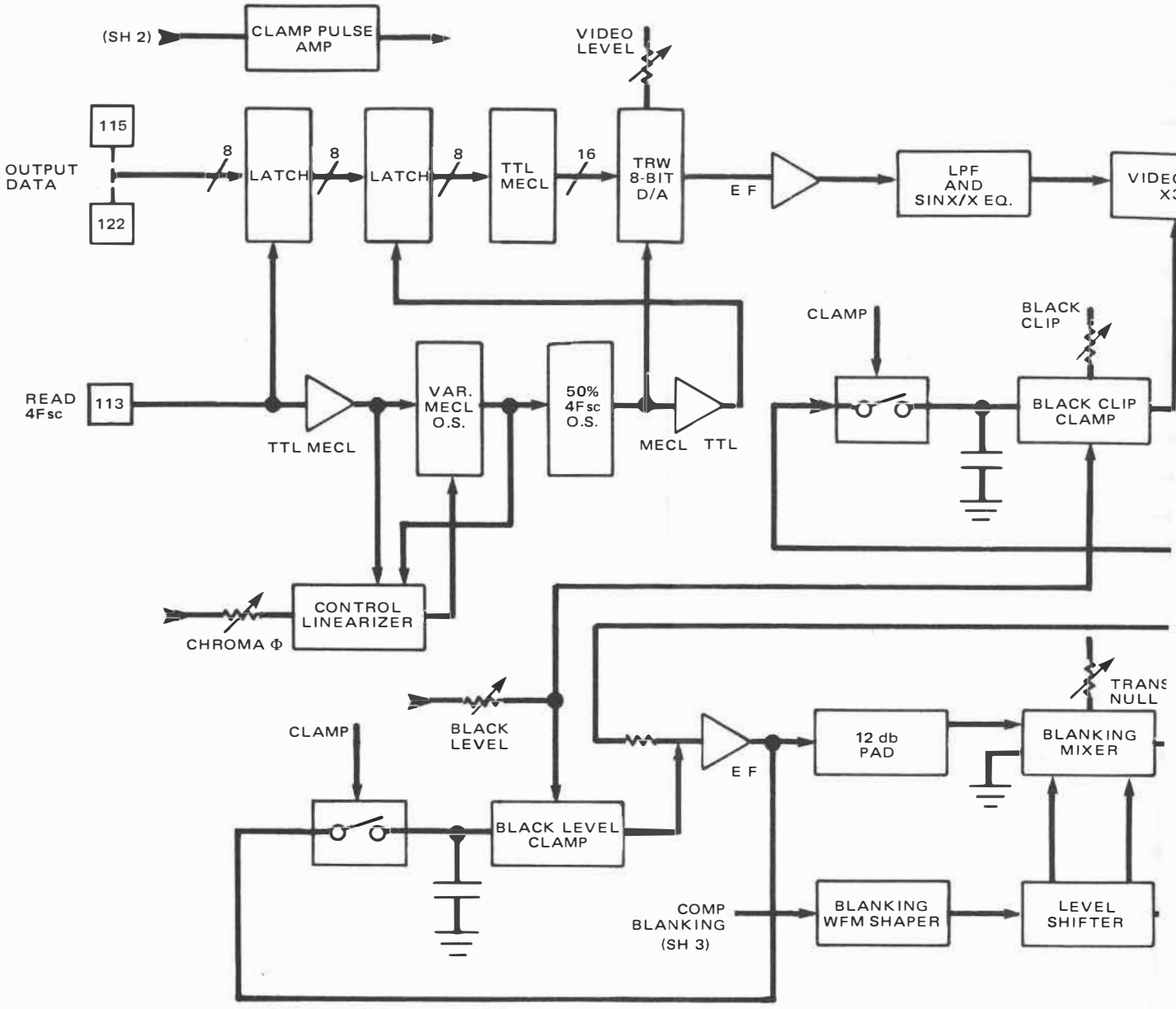
BURST LEVEL
BURST FLAG (SH 3)
BURST ENV SHAPER
MULTIPLIER
SUB-CARRIER (SH 2)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50% 4Fsc O.S.
MECL TTL
BLACK CLIP CLAMP
CONTROL LINEARIZER
CHROMA Φ
TRANS NULL
CLAMP
BLACK LEVEL
E F
12 db PAD
BLANKING MIXER
BLACK LEVEL CLAMP
COMP BLANKING (SH 3)
BLANKING WFM SHAPER
LEVEL SHIFTER

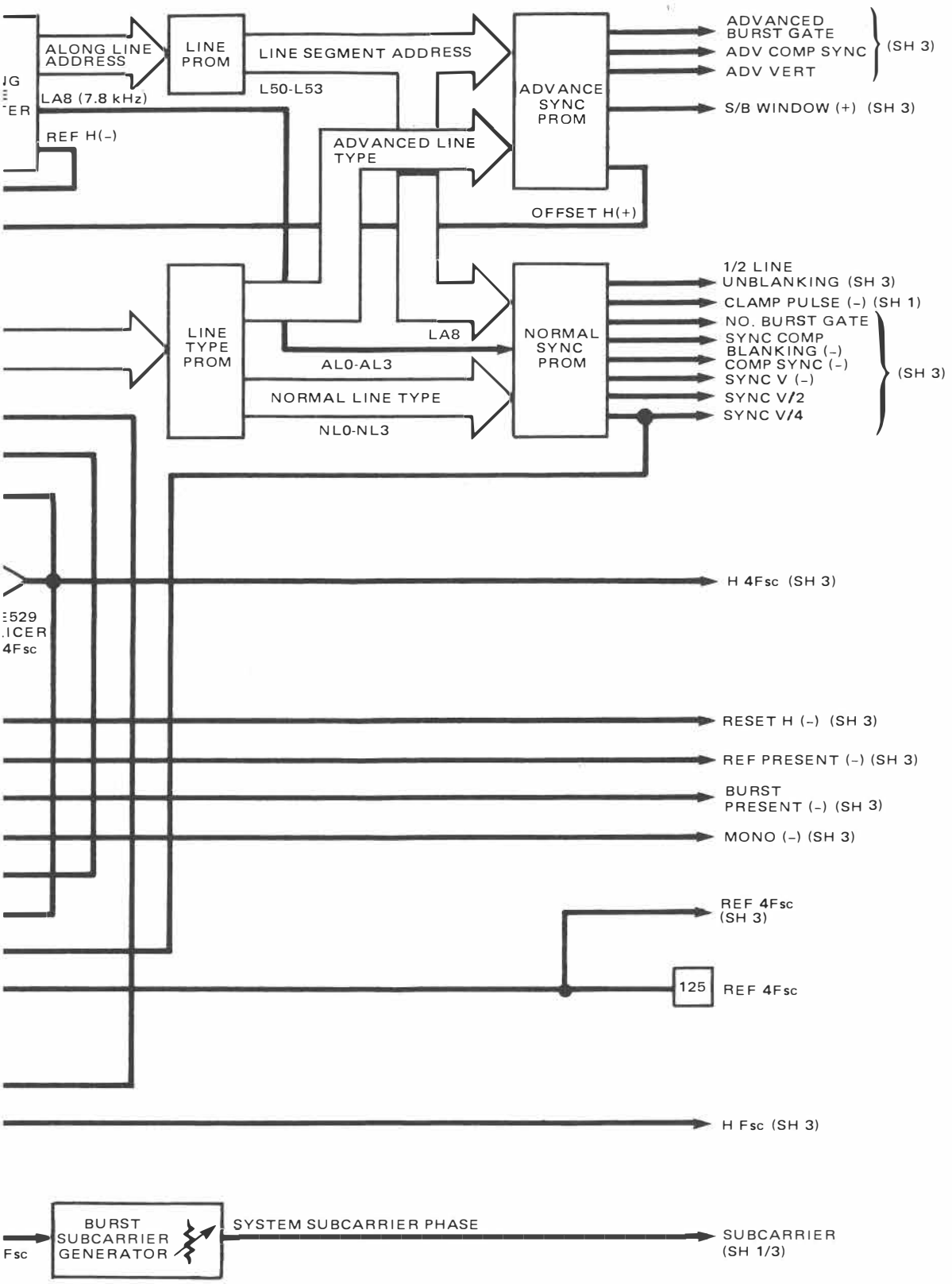
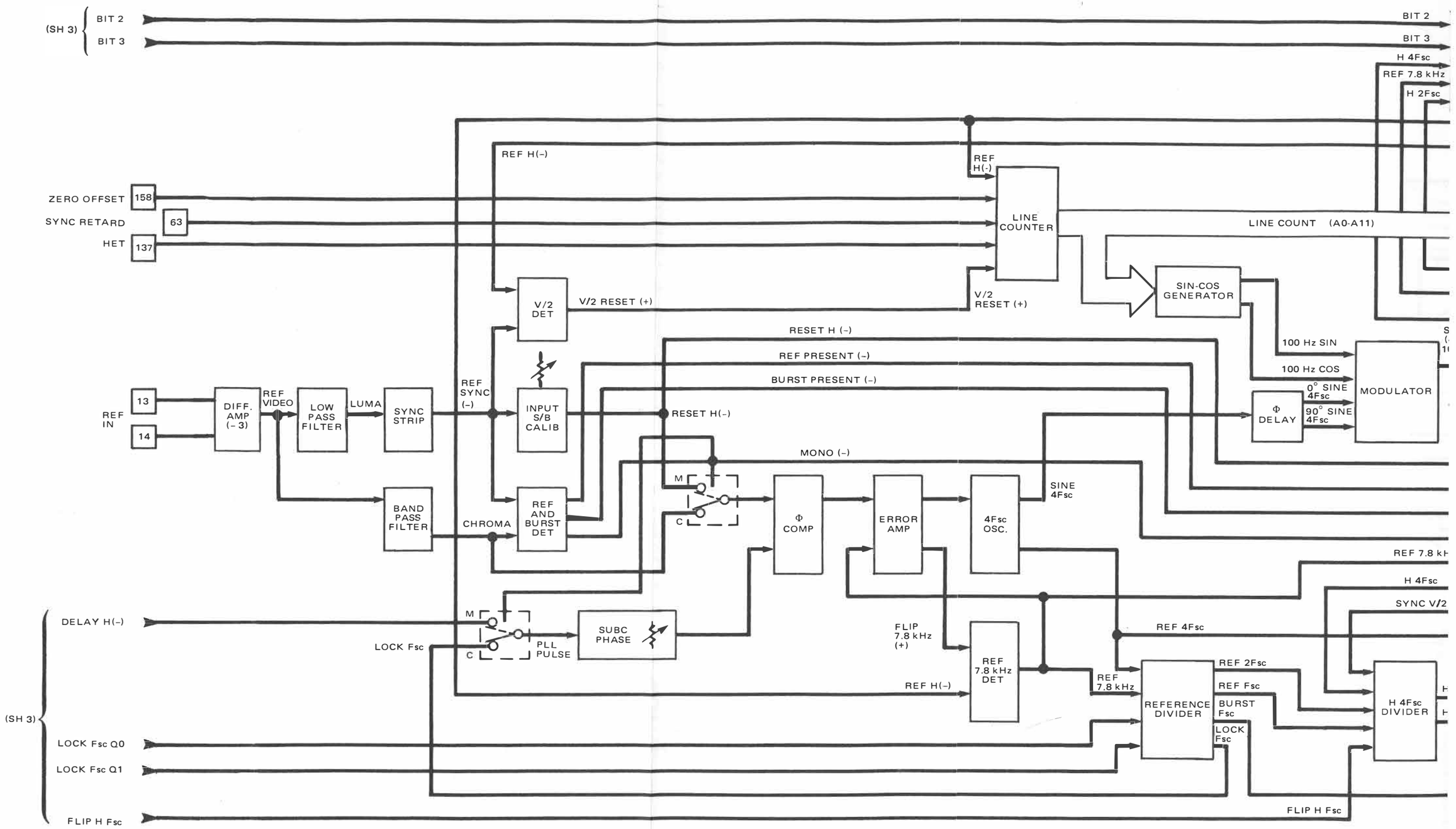


Figure 2-8.
Video Output PWA,
Simplified Block Diagram
(Sheet 2 of 3)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BIT 2
BIT 3
BIT 2
BIT 3
H 4Fsc
REF 7.8 kHz
H 2Fsc
REF H(-)
REF H(-)
ZERO OFFSET
158
SYNC RETARD
63
HET
137
LINE COUNTER
LINE COUNT (A0-A11)
SIN-COS GENERATOR
V/2 DET
V/2 RESET (+)
V/2 RESET (+)
RESET H (-)
REF PRESENT (-)
BURST PRESENT (-)
100 Hz SIN
100 Hz COS
0° SINE 4Fsc
90° SINE 4Fsc
Φ DELAY
MODULATOR
REF IN
13
14
DIFF. AMP (-3)
REF VIDEO
LOW PASS FILTER
LUMA
SYNC STRIP
REF SYNC (-)
INPUT S/B CALIB
RESET H(-)
MONO (-)
M
C
BAND PASS FILTER
CHROMA
REF AND BURST DET
Φ COMP
ERROR AMP
4Fsc OSC.
SINE 4Fsc
REF 7.8 kH
H 4Fsc
SYNC V/2
DELAY H(-)
M
C
LOCK Fsc
PLL PULSE
SUBC PHASE
FLIP 7.8 kHz (+)
REF 4Fsc
REF 7.8 kHz DET
REF 7.8 kHz
REF H(-)
REFERENCE DIVIDER
REF 2Fsc
REF Fsc
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LOCK Fsc
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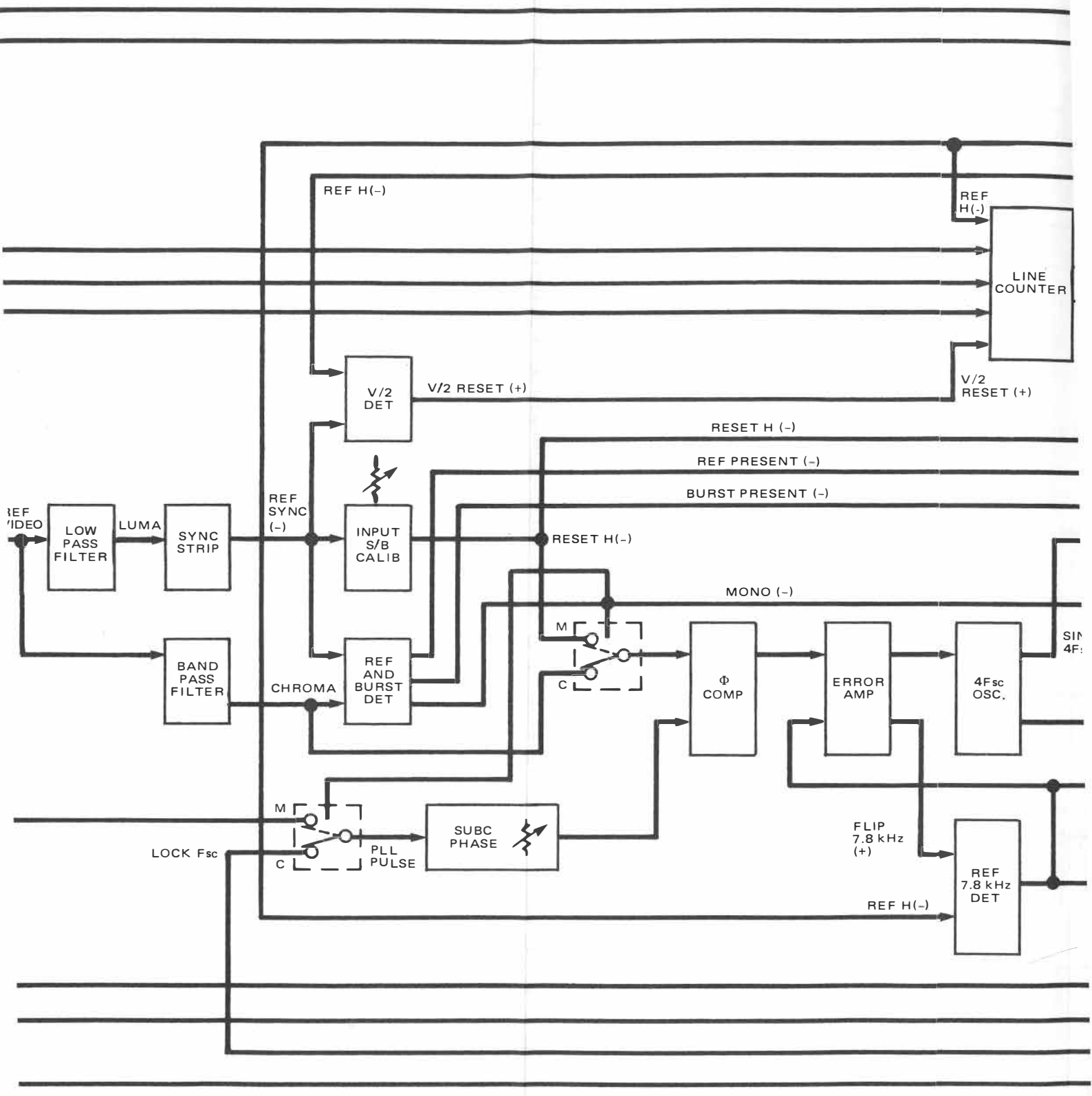
(SH 3)
LOCK Fsc Q0
LOCK Fsc Q1
FLIP H Fsc
FLIP H Fsc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REF H(-)
LINE COUNTER
V/2 DET
V/2 RESET (+)
V/2 RESET (+)
RESET H (-)
REF PRESENT (-)
BURST PRESENT (-)
REF VIDEO
LOW PASS FILTER
LUMA
SYNC STRIP
REF SYNC (-)
INPUT S/B CALIB
RESET H(-)
MONO (-)
M
C
BAND PASS FILTER
CHROMA
REF AND BURST DET
Φ COMP
ERROR AMP
4Fsc OSC.
SIN 4F
M
C
LOCK Fsc
PLL PULSE
SUBC PHASE
FLIP 7.8 kHz (+)
REF 7.8 kHz DET
REF H(-)

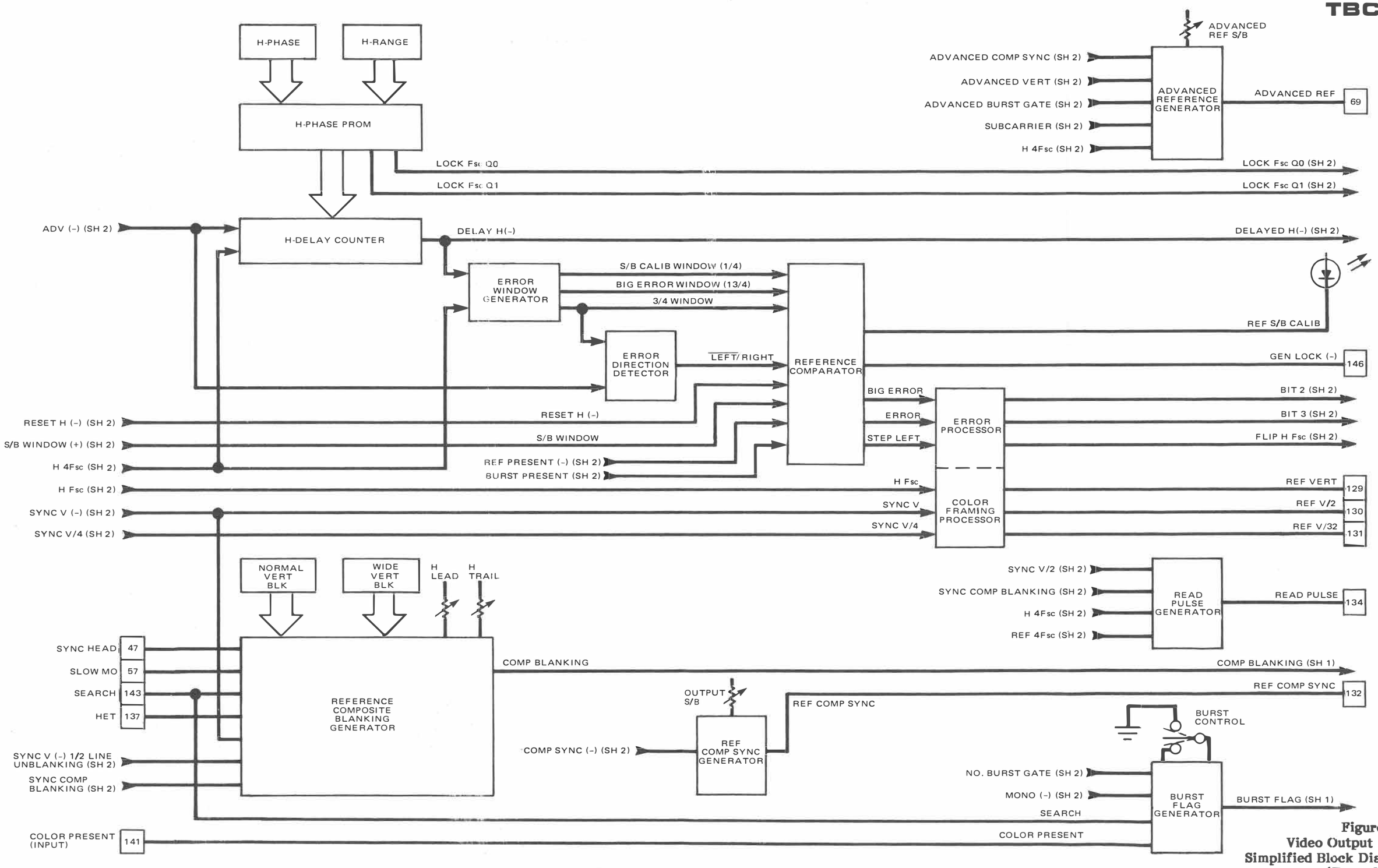
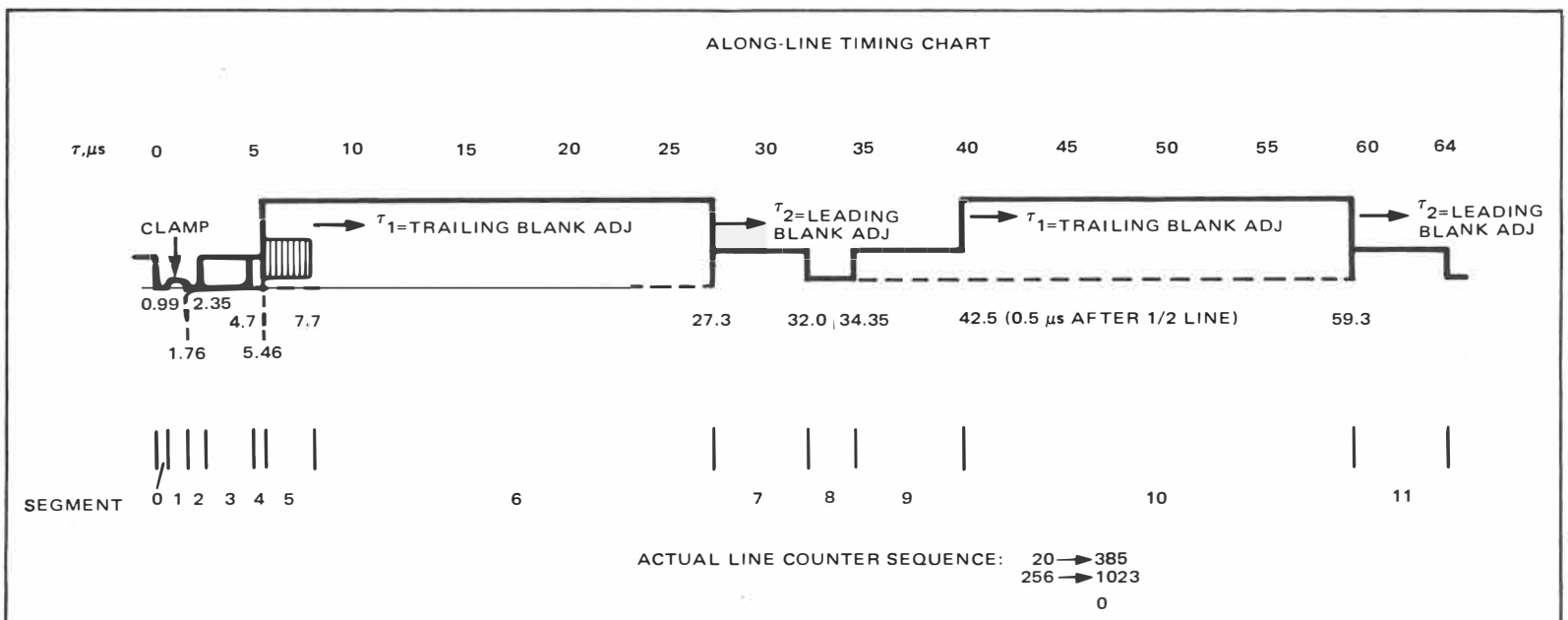


Figure 2-
Video Output PW
Simplified Block Diagra
(Sheet 3 of

Table 2-1. Line Counter Sequence



Segment Number	Transition Timing Beginning of Segment	Operation	Segment Number	Transition Timing Beginning of Segment	Operation
0	0.0	H sync (trailing)	6	7.7	Burst gate (falling)
1	.99	Clamp pulse (rising)	7	27.3	Broad pulse (rising)
2	1.76	Clamp pulse (falling)	8	32.0	Equalizing pulse (falling)
3	2.35	Equalizing pulse (rising)	9	34.35	Equalizing pulse (rising)
4	4.7	H sync (rising)	10	42.5	Blanking timing (trailing)
5	5.46	Burst gate (rising)	11	59.3	Blanking timing (leading)

The reference Fsc is routed to the reference divider from which four Fsc signals are generated each with a 90° phase difference. The burst swing, having been detected in the reference 7.8 kHz detector, generates the 7.8 kHz that is used to modulate (supply burst swing to) the previously mentioned four Fsc signals. An error amplifier monitors the error voltage and when a large voltage swing is detected, every line the TBC burst swing (generated from 7.8 kHz) is out of phase with the reference burst swing and the 7.8 kHz is inverted. After the burst swing has been inserted, the lock Fsc Q signals select one of the four modulated Fsc signals as directed by the H phase control setting. The selected signal becomes the lock Fsc signal and is one input to the phase comparator (reference burst being the other input). Thus the signal selected (lock Fsc) should always be in phase with reference burst.

2-41 Error Window Generation

Three error windows are generated (1/4Fsc, 3/4Fsc, and 13/4Fsc) from the delay-H pulse and, by determining where reference-H falls with respect to the error windows, signals can be generated that reflect the relative position of delay-H to reference-H. The reference comparator outputs are big error (outside 13/4Fsc window), error (inside 13/4Fsc window but outside 3/4Fsc window), and step left (direction).

When reference-H is within the one 4Fsc window, the REF S/B CALIB lamp is lit and the system is color framed. As long as reference-H remains within the 3/4Fsc window the generator will not rephase and the genlock lamp will light. When reference-H is within the 13/4Fsc window, the circuit aligns the delay-H to reference-H by using bit 2 and bit 3 signals to the ALC and by using flip Fsc to reestablish the reference color frame. The 3/4Fsc and the advance-H inputs to the error direction detector generate the signal that establishes the direction that the window must move to align reference-H and delay-H. In the event the reference-H does not fall within the 13/4Fsc window, the error processor outputs bit 2 and bit 3 signals every line until reference H is again within the 3/4Fsc window.

2-42 Color Framing Processor

The color framing processor utilizes H-Fsc, sync-V and sync-V/4 to establish the reference color frame and lock the read side of memory by properly phasing reference V/32.

Reference Fsc and reference 2Fsc signals are routed to the previously discussed H-4Fsc divider. The burst Fsc is sent to the burst subcarrier generator where system subcarrier phase may be adjusted and the subcarrier routed onto the video circuits.

2-43 Advance Reference Circuit

The advance reference circuit provides a VTR advance signal from the TBC to recorders that do not have advance circuitry. The advance is used to establish VPR advance of vertical sync and is required to center the TBC memory read/write relationship within the TBC window.

2-44 Read Pulse Generator

The read pulse generator supplies a read pulse that allows accurate reading of information in the memory. The read pulse generator rephases the sync composite blanking signal with reference 4Fsc in order to establish an H coherent start-read reference.

2-45 Video Processing

The output video processing section receives serial data from the Memory System PWA, and clocks it into the input latch using the read 4Fsc clock. Chroma phase is accomplished by introducing a fixed delay between read 4Fsc and the 4Fsc signal sent to the D/A converter. Latched data bits are applied to the D/A converter and on to a buffer amplifier. A sine X/X equalizer following the D/A converter provides compensation for sampling and flattens the video frequency response. Video is then passed through a low-pass filter, buffered, and the black level is clamped. A chroma bandpass filter and analog multiplier circuit allow setting output chroma gain. The resulting signal goes to a black clip and is then sent to a blanking mixer. Composite blanking is generated in the reference composite blanking generator, utilizing the signal shown on the block diagram, and is then combined with processed video.

Blanked video is supplied to the inputs of two summing amplifiers. These amplifiers also receive composite sync and burst information which is combined with the blanked video. The buffered output of the summing amplifiers goes, via 75Ω line drivers, to VIDEO OUT 1 and VIDEO OUT 2 outputs.

The reconstituted analog video, sync, and burst are mixed in the output video amplifiers to produce a composite video signal which is time-base corrected and delivers a 1-Vp-p signal into a 75Ω impedance to coaxial jacks at the rear panel of the TBC.

SECTION 3
MAINTENANCE

3-1 INTRODUCTION

The following paragraphs provide field maintenance information and alignment procedures applicable to the PAL version of the TBC-6 Digital Time-Base Corrector, Ampex Part Number 1451605. Refer to Section 2, *Theory of Operation*, for details describing functional operation of the TBC-6 circuits.

3-2 PREVENTIVE/PERIODIC MAINTENANCE

Apart from keeping the unit free of dust, which could contribute to heat buildup, the TBC-6 does not require preventive maintenance.

3-3 MAINTENANCE ACCESS

The TBC-6 consists of four large PWA assemblies installed in slots in a card cage enclosure, which provides interconnection at the board edges via a motherboard or backplane interconnect. All PWAs are interchangeable from slot to slot. The top cover of the enclosure is easily removed by taking out the four corner screws, making it convenient to install the PWA intended for alignment in the top slot when performing testing. This precludes the need for an extender board when bench-testing the TBC-6.

The power supply is accessible at the left side of the enclosure when the top cover is removed and the four PWAs are taken out.

3-4 TEST EQUIPMENT REQUIREMENTS

Test equipment suggested for testing and aligning the TBC-6 is listed in Table 3-1. Test equipment with equivalent or better specifications can be substituted for that listed in the table.

Table 3-1. Test Equipment

Equipment	Type/Functions
Digital voltmeter	DC voltage accuracy ± 0.1. Voltage range 100 mV to 20V. Hewlett Packard 3435 or equivalent.
Waveform monitor	Dual-channel, A-B signal subtraction mode. Tektronix 1481 or equivalent.

(Continued next page)

Table 3-1. Test Equipment (Continued)

Equipment	Type/Functions
Vectorscope	Composite video and vector displays, differential gain and phase mode, external and internal phase reference, Tektronix 521A or equivalent.
Signal sources	Color bars, color black (switchable R-Y, B-Y components), variable setup level, 0-50% APL flat field, locked/unlocked subcarrier, modulated/ unmodulated ramp, unmodulated stairstep, Tektronix 148 or equivalent.
Color video monitor	Monitor for viewing PAL standard video. Tektronix 651, or equivalent.
Extender	Ampex Part No. 1451725.
Tuning tool	Technitool AF-12H or equivalent.

3-5 Test Equipment Setup

Field testing presented in this manual suggests use of a composite video test source for reference video and tape video, as illustrated in Figure 3-1. The VTR interconnect should be used to maintain configuration integrity of the TBC and to provide mode switching from the VTR. This method isolates the TBC from possible VTR video signal inaccuracy. VTR tape video output is required for some tests; these alternate setups are shown with broken lines.

Note

Be sure to observe proper use of loop-throughs, equal cable lengths, and terminations as illustrated.

The full complement of test equipment is not always used. Use of a particular instrument is called out where required in the procedure.

3-6 SYSTEM ALIGNMENT AND TESTING

Field testing of the TBC-6 cannot provide complete isolation of each PWA from system interactivity, as is the case in factory testing. It is helpful to remain aware of the functional signal paths as they proceed from board to board and from input to output, as they determine the order in which certain adjustments are made.

The alignment procedures in this section should not be considered as routine maintenance. Rather, they are a means of returning the TBC-6 to normal operation following repair, or possibly to adapting the system to other VTRs or nonstandard facility requirements.

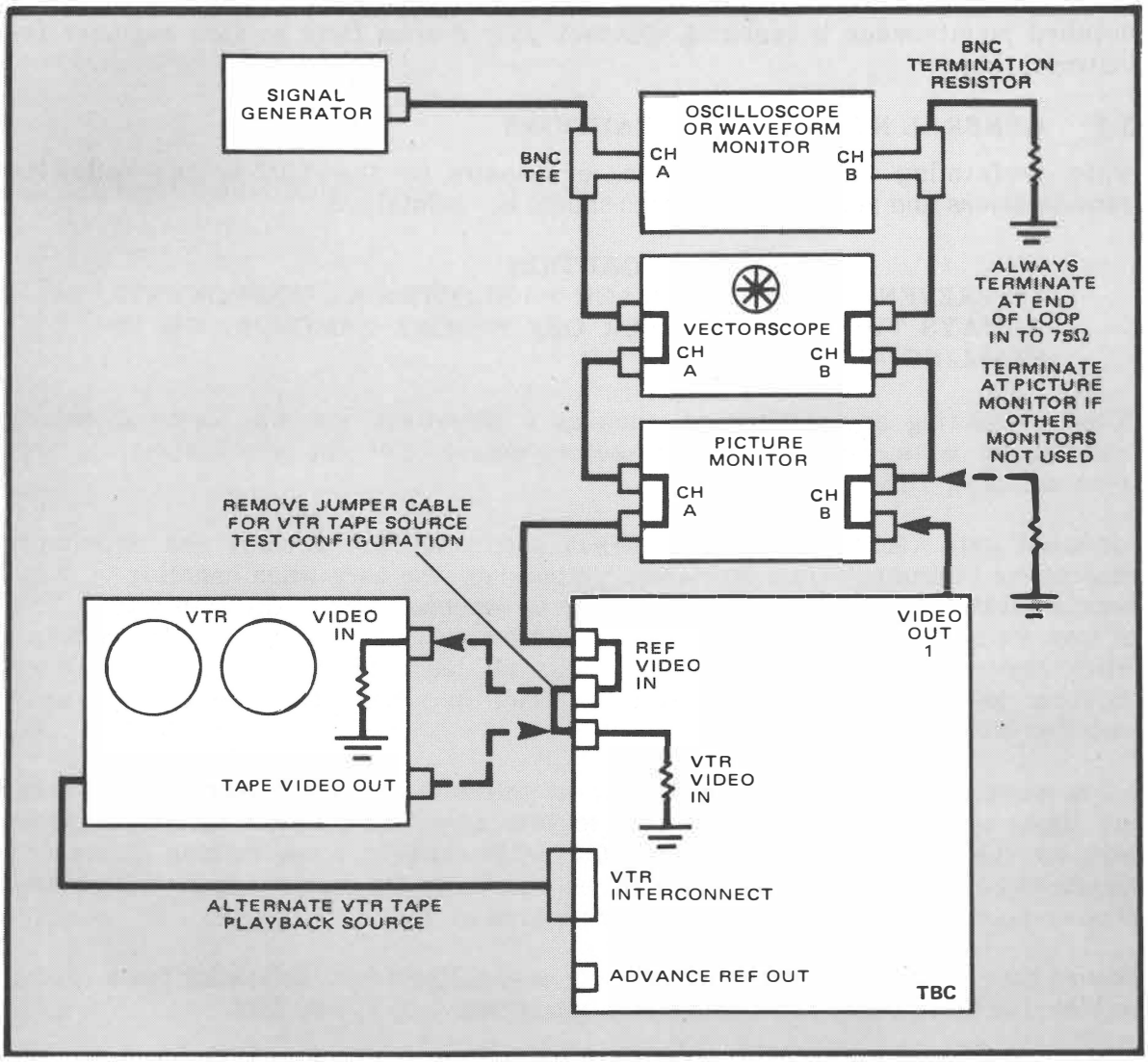


Figure 3-1. Test Equipment Setup

Results indicated in the procedures define normal operating parameters of the TBC-6. To isolate faults, make checks at points described in the procedures and check the waveform/voltage levels given. During such checks avoid unnecessary adjustments, as many of the controls are used to trim circuit tolerances at the time of manufacture and are not intended for field adjustment.

A complete alignment is neither necessary nor recommended. Typically, most adjustments can be confined to the PWA which has experienced repair or component replacement.

In the event that a checkout procedure has a verification step, and upon checking the condition cannot be verified, the preceding steps should be repeated. If this

does not clear the condition, realignment will not clear the problem and more detailed maintenance is required. Contact your Ampex field service engineer for instructions.

3-7 GENERAL NOTES AND PRECAUTIONS

When performing tests, adjustments, or repairs on the TBC-6, the following considerations and general precautions should be maintained.

CAUTION
TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS, ALWAYS TURN TBC-6 POWER OFF BEFORE REMOVING OR INSTALLING ANY PWA.

When connecting any instrument, such as a waveform monitor, vectorscope, or oscilloscope to a video output connector, ensure that the video signal is terminated, using a 75Ω termination.

Insulated gate (MOS/CMOS) field-effect semiconductor devices are extremely susceptible to damage from static-charge buildup. Use care when handling to avoid possible static-charge damage to the device, especially when the humidity is 30% or less. Persons handling such devices should be grounded through a 1-MΩ resistor. When replacing these devices, ensure that all leads of the device are shorted together (usually by the conductive material in which they are packed) until installed into the PWA.

All pulse width measurements are made at the 50% amplitude level. All rise and fall times are measured from the 10% to 90% amplitude levels. All scope probes used to view waveforms should be 10:1 ratio probes. When making dual-trace measurements the probe lengths should be equal. All input and output video signal measurements are taken with signals terminated by 75Ω.

Ensure that jumpers are returned to their original positions following tests. Refer to the complete jumper list in Section 5 (paragraph 5-2) as required.

3-8 PRELIMINARY GUIDELINES

Consult this check-list before beginning any alignment of the TBC-6.

1. Always install the TBC-6 power jumper to reflect the line voltage requirement.
2. Always perform a visual mechanical inspection of all accessible assemblies for any apparent physical damage before beginning any alignment.
3. Ensure that any signal input to REF VIDEO IN and VTR VIDEO IN jacks conforms to EBU input standards, and DS1 on Video Output PWA is lighted according to the procedures of paragraph 3-13.
4. Verify that all front panel controls are set to unity gain.
5. On Memory System PWA, verify that horizontal position switch S3 is set to 8.

6. Power supply voltages should always be within tolerance before any adjustment is made.

3-9 SYSTEM ADJUSTMENTS

System adjustments include power supply adjustments, unity gain adjustment, system phase adjustment, and velocity compensation adjustment.

3-10 Power Supply Check and Adjustment

The power supply system does not require routine adjustment and should not be adjusted unless a need has been established. Usually adjustment is required if a power supply module has been replaced. Prior to making an adjustment, perform the power supply check procedure.

3-11 Power Supply Check

Before proceeding with alignments, or if power supply problems are suspected (or have been corrected), a check of the individual supply voltages can be made at the Motherboard PWA pins. Check the power supply voltages under typical line voltage conditions and with all PWAs installed.

Proceed as follows:
With unit top cover removed, turn on the TBC power and check the regulated voltages given below, using a digital voltmeter.

Voltage (pins)	Measurement	Location/ Adjustment
+12V (5—8)	+12.00V ±0.1V	A4/R1
-5V (87—88)	-5.20V ±0.1V	A5/R23
-12V (93—96)	-12.00V ±0.1V	A6/R12
+5V (105—107,193—196)	+5.0 ±0.1V	A10/R16
Ground (1—4)	N/A	

Note

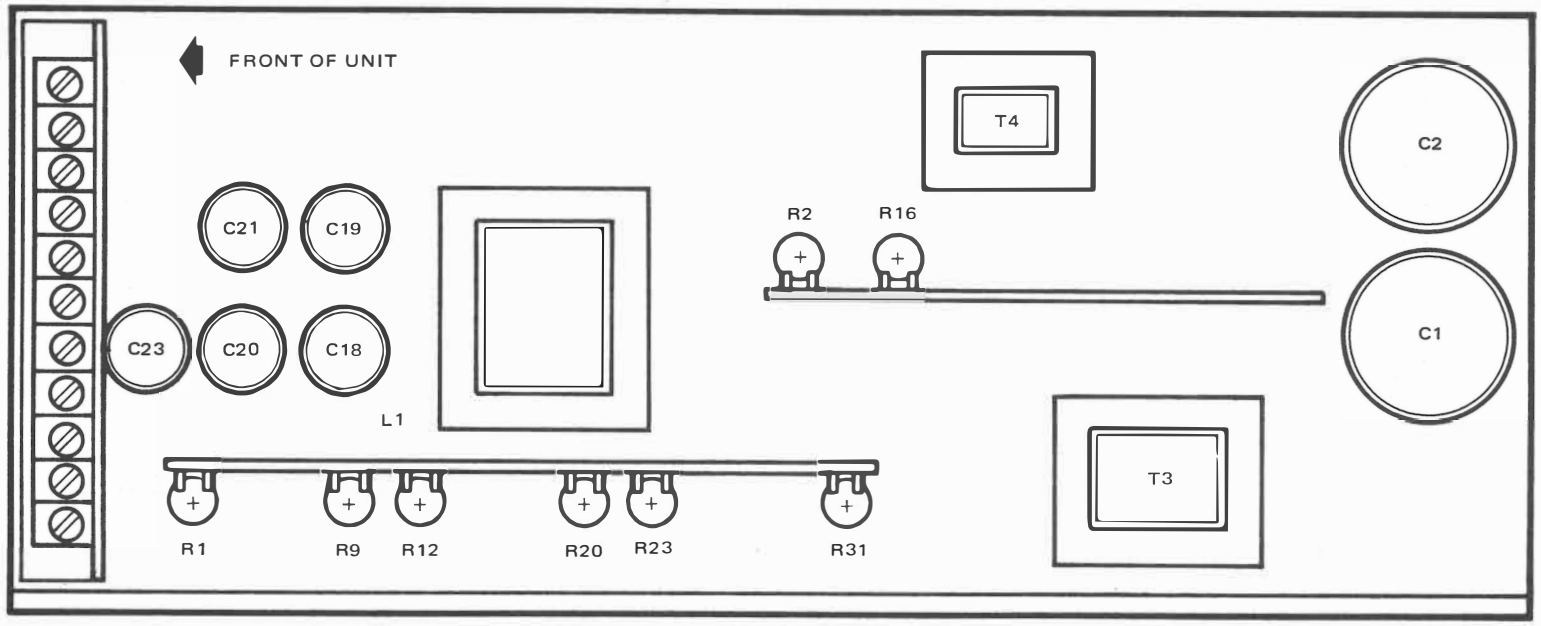
Any gross deviation from the voltage tolerance may indicate a fault (such as an overload on one of the PWAs), or that the power range jumper is not selected for available line voltage.

3-12 Power Supply Adjustment

STEP 1 Adjust appropriate control if measured values only slightly exceed tolerances shown. To reach adjustments, turn off main power and remove all PWAs. This allows access with a screwdriver from inside chassis. See Figure 3-2.

STEP 2 Verify that generator noise on all supplies is less than 75 mV and that there are no spikes above 150 mV.

Figure 3-2. Power Supply Access



R1 + 12 VOLTAGE ADJUST TB1-4
R9 + 12 CURRENT LIMIT ADJUST
R12 – 12 VOLTAGE ADJUST TB1-6
R20 – 12 CURRENT LIMIT ADJUST
R23 – 5.2 VOLTAGE ADJUST TB1-5
R31 – 5.2 CURRENT LIMIT ADJUST
R2 + 5 CURRENT LIMIT ADJUST
R16 + 5 VOLTAGE TB1-10, 11

NOTES: ALL VOLTAGES ARE SET WITH A ±0.03V TOLERANCE EXCEPT FOR THE + 5V SUPPLY AND IT IS SET WITH A ±0.05V TOLERANCE.

CHASSIS GROUND IS TB1-1, VOLTAGE COMMONS ARE TB1-7, 8, 9

ALL SUPPLIES ARE 4 AMP SUPPLIES EXCEPT THE + 5V SUPPLY AND IT IS A 25 AMP SUPPLY.

PICTORIAL SAME SIDE AS THE POWER SUPPLY FACING CARD RACK

3-13 SYSTEM PHASE ADJUSTMENT

Use the following procedure to adjust TBC-6 subcarrier and horizontal phase to match EBU standard PAL house reference. Figure 3-3 shows location of controls on Video Output PWA.

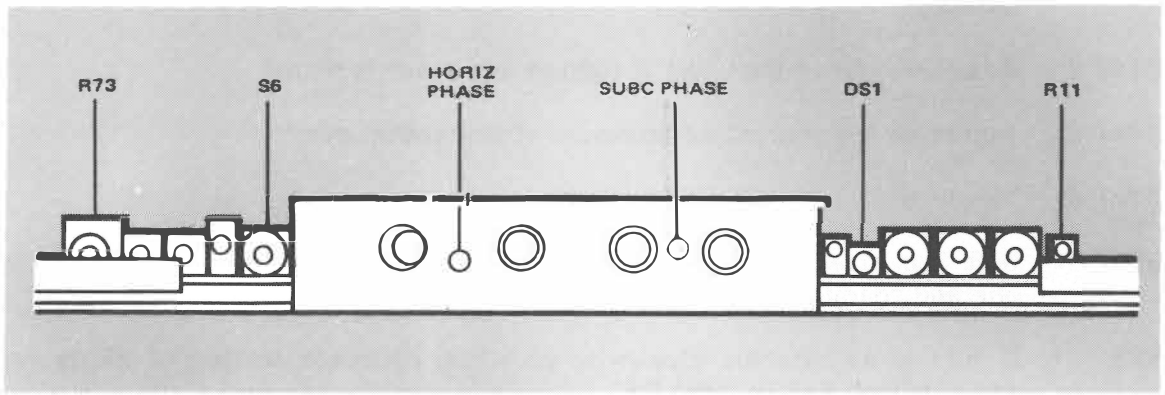


Figure 3-3. Video Output PWA Adjustment Locations

STEP 1 Connect PAL house reference to waveform monitor A input, looping through TBC-6 REF VIDEO IN connector. See Figure 3-4.

STEP 2 If reference video input is EBU standard, ensure that jumper J1 on the Video Output PWA is in A-B position. If non-EBU standard TBC output video is present, place jumper P1 in position A-C.

STEP 3 Connect TBC-6 VIDEO OUTPUT 1 output to waveform monitor B input. Set waveform monitor for A-B display.

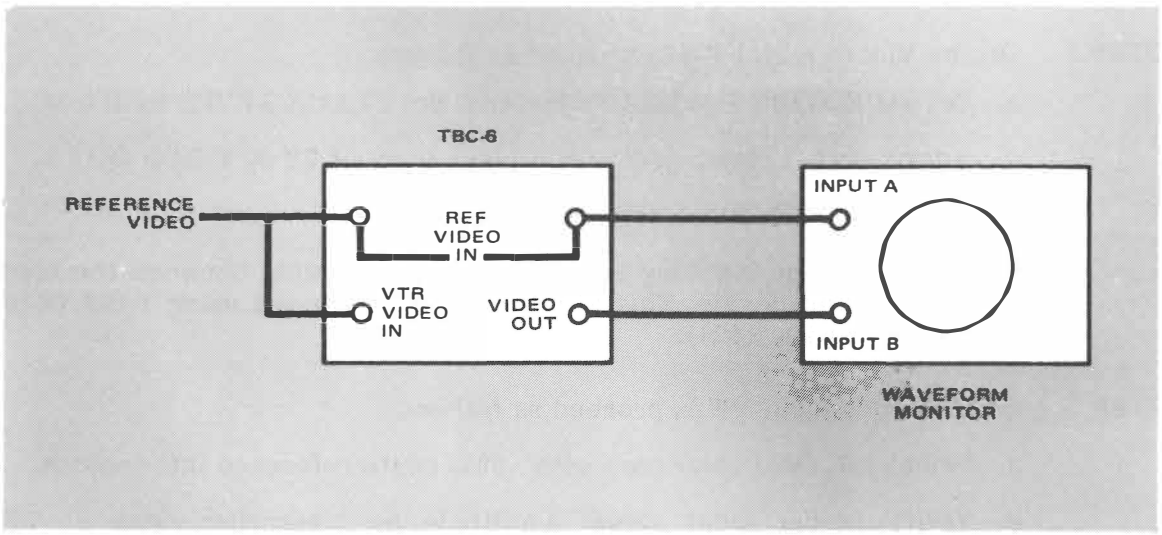


Figure 3-4. Phase Adjustment Setup

STEP 4 Center R11 (input sync/burst calib) on Video Output PWA with green indicator DS1 lighted.

STEP 5 If reference video is nonstandard, center R73 (nonstandard).

STEP 6 Adjust subc phase R380 and horiz phase S5 to null reference and output bursts .

STEP 7 Readjust R11 so that DS1 is lighted and burst is nulled.

STEP 8 Adjust S6 for nearest coincidence of horizontal sync

STEP 9 Readjust R11 so that DS1 is lighted.

STEP 10 If R11 is at extreme counterclockwise position, increase setting of S6 by one and readjust R11 to light DS1.

STEP 11 If R11 is at extreme clockwise position, decrease setting of S6 by one and readjust R11 to light DS1.

STEP 12 If reference video is nonstandard, adjust R73 for horizontal sync coincidence.

3-14 Unity Gain

In order to properly set up unity gain on the TBC-6, the preliminary adjustments should be done on the Video Output PWA, then the Video Input PWA. The final adjustment is then done on the Video Output PWA. The following steps describe the proper sequence.

STEP 1 Connect a DVM to TP5 on the Video Input PWA. Adjust R193 on the Video Input PWA for exactly -2.00V.

STEP 2 On the Video Output PWA, proceed as follows:

a. Set VIDEO OUT LEVEL to minimum. Set BLACK LEVEL to detent.

b. Adjust output clamp R421 for a black level of 0V at VIDEO OUT 1.

c. Return VIDEO OUT LEVEL to detent position.

d. Verify that no blanking transition glitch is visible between the black and blanking levels. This glitch can be minimized using R106 (R106 interacts with R421).

STEP 3 On the Video Input PWA, proceed as follows:

a. Select full field color bars with 100% white reference into input A.

b. Verify proper input signal amplitude by measuring video at TP7 (714 mV between peak white and pedestal).

c. Verify that output vectors displayed on vectorscope do not break up when video level control R218 is adjusted through entire range. If not proceed to step d.

d. Readjust R161 and R162 on Video Input PWA and repeat step c.

e. Adjust video input gain R200 for 1.10V between peak white and pedestal at the video on TP4.

f. Adjust A/D clamp R463 for a black level of 0V at VIDEO OUT 1.

Note

As VIDEO OUT LEVEL is rotated throughout its range, the signal at VIDEO OUT 1 should fade to the blanking value which is at 0V.

STEP 4 On the Video Output PWA, proceed as follows:

a. Set VIDEO OUT LEVEL to detent.

b. Adjust video level unity R384 for unity gain throughout the system.

c. Install the Video Output PWA in the top slot.

d. Adjust as desired during playback (S1—PLAY, S2—SLOW).

e. Set output burst select switch S7 on Video Output PWA as desired.

3-15 Burst/VCO A/D Ramp

STEP 1 On Tape Clock PWA connect channel 1 scope probe to view the A/D input at TP43. Use U98-9 (tape vert) for scope sync. Set time base at approximately 2 ms/div. Adjust control R262 to obtain a tri-level waveform as shown in Figure 3-5.

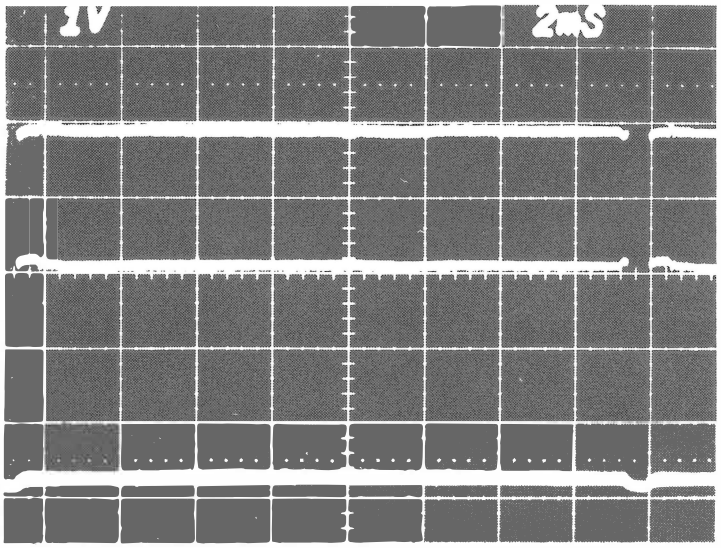


Figure 3-5. Tri-Level Waveform

STEP 2 Tri-level waveform should display levels of +0.1V and +1.9V for the upper two levels of the waveform. If not proceed to step 3.

STEP 3 Adjust offset control R167 and gain control R87 to obtain levels of +0.1V and +1.9V for the upper two levels of the waveform. The lowest level of the waveform should be at approximately -2.5V, but this is not critical.

3-16 Velocity Compensation Gain and Quadrant Discriminator

STEP 1 On Memory System PWA connect channel 1 of scope probe to view A/D output at TP4.

STEP 2 Observe video from MONITOR VIDEO OUT on channel B of vector scope.

STEP 3 Adjust R262 on Tape Clock PWA (first potentiometer on the left front of Tape Clock PWA) to produce quadrant jumps (TP4—0.1V to -1.9V, toggling). This is displayed as two sets of vectors that are offset in phase with a single burst vector. A slight adjustment of R59 may be necessary to observe this.

STEP 4 Adjust R59 line-error gain to align two bright dots of blue vector into one bright dot as seen on vectorscope.

STEP 5 Adjust R28 and R29 to align 90° light dots with bright dot.

STEP 6 Repeat steps 4 and 5 until good vector alignment is obtained.

STEP 7 Position yellow dot in proper square on vectorscope. Adjust R60 offset adjustment, to center blue dot in its square.

Note

The adjustment of R60 has a significant effect on differential phase and can be used to set differential phase using a modulated ramp signal.

STEP 8 Set NORM/HET (MODE SW) to NORM. Play back color bars signal recorded on tape.

STEP 9 Switch vel comp switch S2 (on Memory System PWA) on and off, to verify that velocity compensation circuitry is operational.

STEP 11 With vel comp switch S2 on, adjust R48 vel comp gain for smallest blue dot.

3-17 MEMORY SYSTEM PWA ALIGNMENTS

The memory adjustments consist of a balance adjustment and oscillator peaking adjustment.

3-18 Balance

The balance adjustment aligns the difference amplifier that is used to derive the first order approximation.

STEP 1 On Memory System PWA observe TP4 and set R262 on Tape Clock PWA to 1V ±0.1V.

STEP 2 On Memory System PWA observe U100-1 and adjust R39 for 0V ±0.1V.

3-19 Oscillator Peaking Adjustment

Performing this adjustment optimizes the reference 4Fsc Oscillator.

STEP 1 Adjust L2, oscillator frequency, for a reading of 5V ±0.1V at TP1.

STEP 2 Place scope probes on U136-1 and U136-13.

STEP 3 Adjust R15 for minimum jitter between negatives edges of the two sweeps on scope presentation.

3-20 VIDEO OUTPUT PWA ADJUSTMENTS

The Video Output PWA adjustments consist of the coarse chroma phase adjustment, back porch and burst level, clamp pulse delay, advance reference timing, and signal timing adjustments.

3-21 Coarse Chroma Phase Adjustment

In the chroma phase detent position, the burst-to-chroma phase relationship should be correct. If not, perform the following alignment procedure. This adjustment will affect system timing.

STEP 1 Observe output on a vectorscope.

STEP 2 Adjust burst phase control R239 so that burst-to-chroma phase is correct.

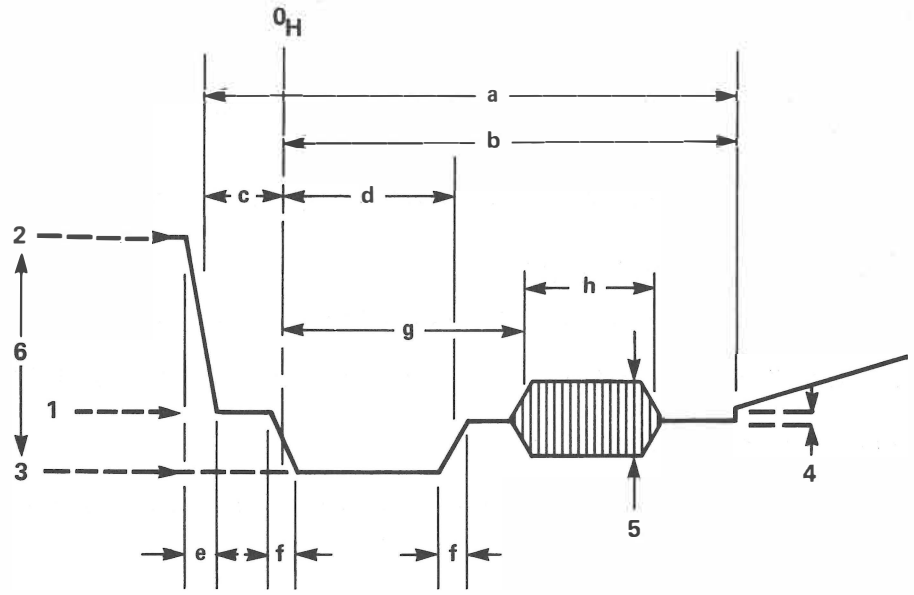
3-22 Back Porch Levels/Burst Level

The dc level for reference blanking (Figure 3-6) should be set for 0.00V during the back porch interval. The burst amplitude is to be set for 40 IRE.

STEP 1 Select 75% amplitude test signal (color bars) with 0% setup and 75% white reference calibration pulse.

STEP 2 Connect oscilloscope to VIDEO OUT 1 and trigger from U139-9 which is REF H signal.

STEP 3 Adjust burst level control R47 fully counterclockwise and note that burst amplitude on the oscilloscope is reduced to zero.



SIGNAL LEVELS		1 UNIT = 10 mV
1	BLANKING REFERENCE	30 UNITS
2	PEAK WHITE	100 UNITS = 1.0V
3	SYNCHRONIZING	0 UNITS = 0.0V
4	PEDESTAL	0 UNITS
5	PEAK-TO-PEAK BURST	30 ±4 UNITS = 0.3 ±0.03V
6	PEAK-TO-PEAK VIDEO	100 UNITS = 1 Vp-p

SIGNAL TIMING		µs
a	LINE BLANKING INTERVAL	12 ±0.3
b	OH TO END OF BLANKING	10.5
c	FRONT PORCH	1.5 ±0.3 (1 = 1.65 ±0.1)
d	SYNC PULSE	4.7 ±0.2
e	RISE/FALL TIME OF BLANKING	0.3 ±0.1
f	RISE/FALL TIME OF LINE SYNC	0.2 ±0.1 (1 = 0.25 ±0.05)
g	START OF BURST (MIN. BREEZWAY)	5.6 ±0.1 (0.6)
h	DURATION OF BURST	2.25 ±0.25 (10 ±1 CYCLES)

Figure 3-6. 625 PAL (B, G, I Systems) Line Synchronization

STEP 4 Verify that dc level of the back porch interval is 0V. Adjust for zero using reference blanking level control R119.

STEP 5 Adjust burst amplitude for 286 mV, using R47.

Note

Terminate the video signal with 75Ω at the oscilloscope for this procedure. Ideally, a high-accuracy differential plug-in would be used for this measurement.

3-23 SIGNAL TIMING CHECKS AND ALIGNMENT

The paragraphs that follow provide the means to ensure that the different elements of the output video signal comply with EBU standards for their duration and relative delay.

3-24 H-Sync Level

Using sync level control R283, adjust H sync amplitude for 286 mV.

Note

Terminate the video signal with 75Ω at the oscilloscope for this procedure. Ideally, a high-accuracy differential plug-in would be used for this measurement.

3-25 H-Blanking

STEP 1 Connect oscilloscope channel 1 to VIDEO OUT 1 and channel 2 to TP49.

STEP 2 Set H-blanking leading edge and H-blanking trailing edge controls R473 and R474 as desired.

3-26 VIDEO INPUT PWA SETUP

Install the Video Input PWA in the top slot. Verify that the VIDEO IN LEVEL and BLACK LEVEL controls are in their detent position. Verify that MODE SW is set to NORM.

3-27 Monitor Video Level

STEP 1 Connect MONITOR VIDEO OUT to B input of a 7a13 differential plug-in, or equivalent.

STEP 2 Select NORM at MONITOR VIDEO switch. Adjust monitor gain control R119 on Video Input PWA for less than 10 mV difference signal between input and output .

STEP 3 Select BYPASS at MONITOR VIDEO switch. Verify less than 20-mV difference signal between input and output .

Select NORM at MONITOR VIDEO switch when through.

3-28 RF Dropout Detection

STEP 1 Connect subcarrier from the TEK140 through a 20-dB attenuator pad to RF IN.

STEP 2 Set AGC level control R445 to center. Set R434 and AGC range control R461 fully clockwise.

STEP 3 With TBC power off, and using 20-MHz filter on scope, verify 150 mV ± 50 mV at the signal side of R462-39,40.

STEP 4 Turn TBC power on. Set R445 for 500 mVp-p subcarrier measured at TP49.

STEP 5 Turn R461 slowly counterclockwise. Note that the subcarrier at TP49 goes to less than 30 mVp-p.

STEP 6 Turn R461 slowly clockwise. Note that subcarrier goes to more than 500 mV and jumps back to 500 mVp-p. Leave R461 set at point where the jump occurs.

STEP 7 Connect scope channel 1 to U82-12. Set R434 fully counterclockwise, note TTL high for approximately 150 ns with a 280-ns period.

STEP 8 Slowly turn R434 clockwise. Note positive pulse goes to zero. Slowly turn R434 counterclockwise until pulses begin to reappear and picture begins to break up. Turn R434 an extra one-eighth turn clockwise past point where positive pulse goes to zero. There should be no picture breakup.

STEP 9 Disconnect subcarrier and 20-dB pad from the TBC. Play back a known good rf recording. Ensure a good color picture. All colors should be correct.

3-29 TAPE CLOCK PWA ADJUSTMENTS

3-30 Preliminary

STEP 1 Select a split field color bar signal from the video generator. Connect to the REF VIDEO IN and VTR VIDEO IN A inputs, and verify that DS1 on Video Output PWA is on.

STEP 2 Install the Tape Clock PWA in the top slot.

3-31 VCO Frequency and Phase Comparator Alignment

STEP 1 Set VPR-6 for EE operation.

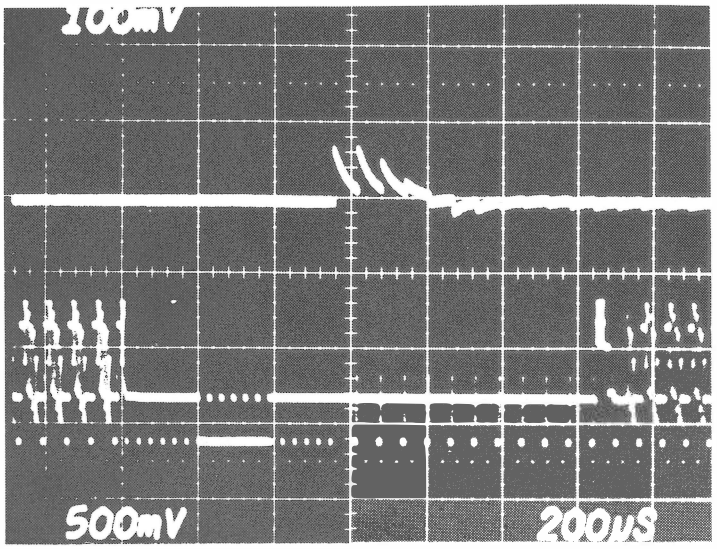
STEP 2 Connect scope probe to TP1 on Tape Clock PWA. Adjust L2 for 4.0V at TP1 (scope accuracy is sufficient).

STEP 3 Connect scope probe to the digital phase comparator input at TP41. Trigger from TP41, positive. Adjust VCO 0 comp range control R270 to obtain a symmetrical square wave with a period of 64 µs.

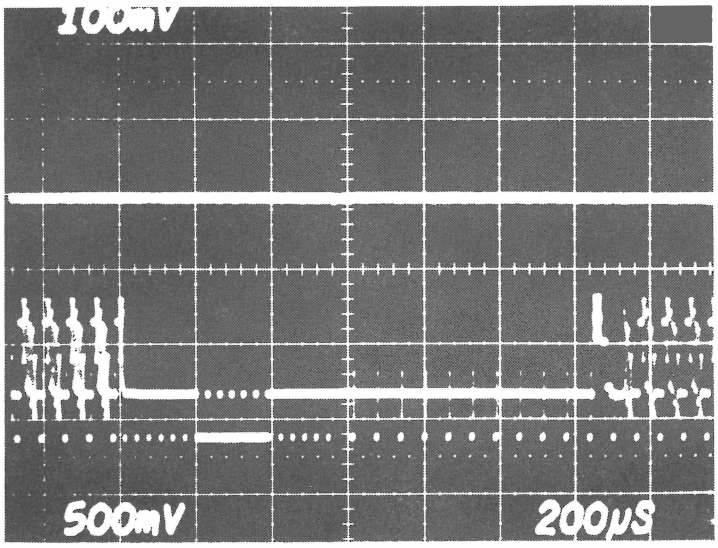
STEP 4 Connect channel 1 scope probe to TP1 on Tape Clock PWA and set for 0.1 V/div, ac-coupled. Monitor output video on channel 2 of scope. Use U98-9, tape vert, as an external scope trigger. Use delayed sweep at approximately 0.2 ms/div to expand display during vertical interval.

STEP 5 Adjust phase comp center control R262 to the center of its range while maintaining good vector quality.

STEP 6 Adjust tape-h reset qualify delay control R269 for a smooth trace through the vertical region as shown in Figure 3-7.



TP1 with R269 Adjusted Too Far Counterclockwise



TP1 with R269 Correctly Adjusted

Figure 3-7. Tape H Reset Qualify

STEP 7 Disconnect output video from channel 2 of the scope. Connect channel 2 scope probe to TP42. Fine tune R269 to obtain a smooth trace through the vertical interval and 1.0V for the upper voltage level at TP42.

Note

If a smooth trace and 1.0V cannot be obtained at the same time, a slight readjustment of R262 may provide necessary range on R269.

STEP 8 Connect channel 1 scope probe to TP18. Connect channel 2 scope probe to TP19. Trigger on channel 1, positive. Verify that the 140-ns pulse on channel 2 is near center of 660-ns pulse on channel 1.

3-32 Shuttle Damping

STEP 1 Install the Tape Clock PWA in the top slot.

STEP 2 Verify that the unit is able to reproduce a monochrome picture when VTR is in full speed forward or reverse shuttle.

STEP 3 Place VTR in shuttle mode. Adjust R53 (error gain) so that horizontal disturbances in vertical boundaries are as smooth as possible with respect to vertical edge at all shuttle speeds.

STEP 4 With VTR in full speed forward shuttle, switch TAPE/EE back and forth several times. Verify lock on and display of a monochrome video signal when off-tape video is selected.

STEP 5 With VTR in full speed reverse shuttle, switch TAPE/EE back and forth several times. Verify that lock is on and a monochrome video signal is displayed when off-tape video is selected.

STEP 6 Place VTR in STOP and EE mode.

STEP 7 Connect scope probe to TP43 and adjust R262 for 1.0V ±0.1V on upper voltage level.

3-33 COLOR FRAMING (WITH VPR-6)

STEP 1 Set up TEK 148 to CCIR standard. Select full field output.

STEP 2 Ensure TBC front panel MODE SW switch is on NORM. On VPR-6, switch color framer on and set NORM/INVERT switch to NORM.

STEP 3 Verify that calibrate control on Tape Clock PWA is in detent position.

STEP 4 Make recording of window test signal.

STEP 5 Play back recording of window test signal.

STEP 6 On the picture monitor, switch the scan switch to pulse cross and the input mode switch to A-B.

STEP 6 Ensure that right-hand green LED is illuminated on the Memory System PWA, EDIT READY is on and INVERT is off.

STEP 7 Verify that the picture is completely cancelled and there are no bright horizontal or vertical lines at border of window.

Note

Ignore the bright vertical and horizontal lines which may appear on the horizontal and vertical sync edge.

STEP 8 Adjust the subc phase control on Video Output PWA for complete color cancellation.

STEP 9 With VTR still in play mode, turn TBC power on and off several times. The unit should color frame each time the power is restored.

3-34 SLOW-MOTION ADJUSTMENTS

The slow-motion adjustments include the decode/encode gain, the V-axis decode compensation and slow-motion vector compensation.

3-35 Decode /Encode Gain

STEP 1 Play back color bars and Y-reference recording in variable play mode at approximately one-half play speed.

STEP 2 Slightly misadjust R45 to obtain dual vector display on vectorscope.

STEP 3 With scope probe connected to TP43, adjust R262 for tri-level waveform.

STEP 4 Adjust R2 and R78 for smallest vector dots with smallest tails.

STEP 5 Readjust R45 for a single set of vectors

STEP 6 With scope probe connected to TP43, adjust R262 for 1.0V ±0.1V on upper voltage level .

3-36 V-Axis Decode Compensation

STEP 1 Place video input PWA on top slot.

STEP 2 Set J16 to A-C to disable the decode Fsc loop.

STEP 3 Play back color bars and Y reference recording in variable play mode.

STEP 4 Adjust R76 and/or R45 on Tape Clock PWA so that single set of vectors is displayed throughout variable speed range.

Note

This may be done by observing vector jitter at both ends of variable play range and adjusting R76 to try to equalize jitter at both ends. Minimize the jitter using R45 across entire range of variable play.

STEP 5 With scope probe connected to U31-7 on Video Input PWA, adjust R314 for 6V ±0.1V.

STEP 6 Set J16 on video input PWA to A-B to restore decode Fsc loop.

STEP 7 Playback color bars and Y reference recording in variable play mode.

STEP 8 Adjust R76 on Tape Clock PWA to make voltage at U31-7 on Video Input PWA as constant as possible throughout variable play range of VTR.

STEP 9 Readjust R45 for most stable vector display with VTR in variable play mode.

STEP 10 If necessary, fine tune R314, R45, and/or R76 to obtain most stable vectors possible and 6V ±0.05V at U31-7 throughout the variable speed range.

Note

There may be some vector phase shift over the variable play range.

3-37 Slow-Motion Vector Compensation

STEP 1 Connect video output of VTR to VIDEO INPUT A of the TBC.

STEP 2 Place the VTR into variable play mode. While playing back a color bar recording in variable play mode, adjust R77 for stationary vectors throughout the slow motion range.

STEP 3 Adjust R46 to properly position the vectors in their respective squares.

STEP 4 Repeat steps 2 and 3 if neccessary.

Note

This is done most easily by adjusting the VTR play speed back and forth between still frame and full forward and noting vector movement for different positions of R77.

SECTION 4
REMOVAL AND REPLACEMENT

4-1 GENERAL

This section describes removal and reinstallation of the TBC-6 replaceable parts. The unit illustrated in this section is shown without a front door assembly, slide members, or trim pieces for clarity.

4-2 REMOVING AND REPLACING COMPONENTS ON THE CARD CAGE

Replaceable components on the card cage assembly consist of filter capacitors and coaxial connectors on the card cage motherboard assembly and the motherboard assembly itself. To replace components on the card cage assembly, the assembly must first be removed from the TBC-6 chassis.

4-3 Card Cage Assembly

Remove card cage assembly as follows:

STEP 1 Release four quarter-turn latches and remove cover. (See Figure 4-1.)

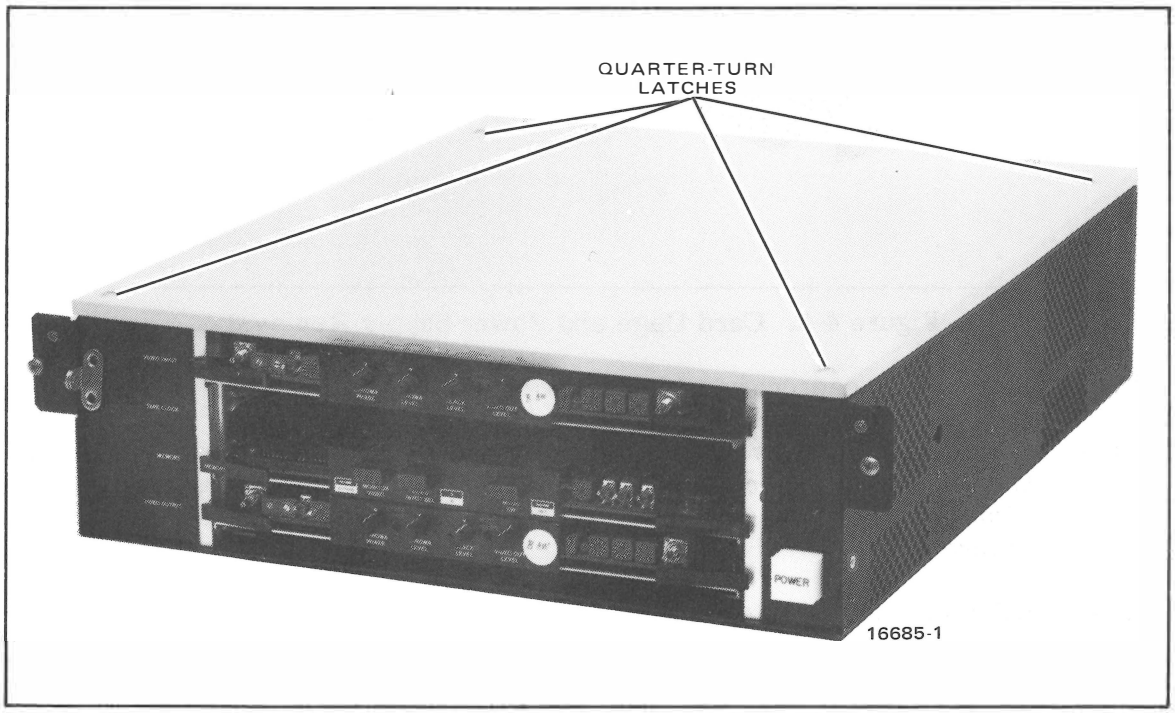


Figure 4-1. Unit Cover Removal

STEP 2 Open front door (not shown) and remove PWAs.

STEP 3 Remove four cross-recessed screws at front of card cage assembly. (See Figure 4-2.)

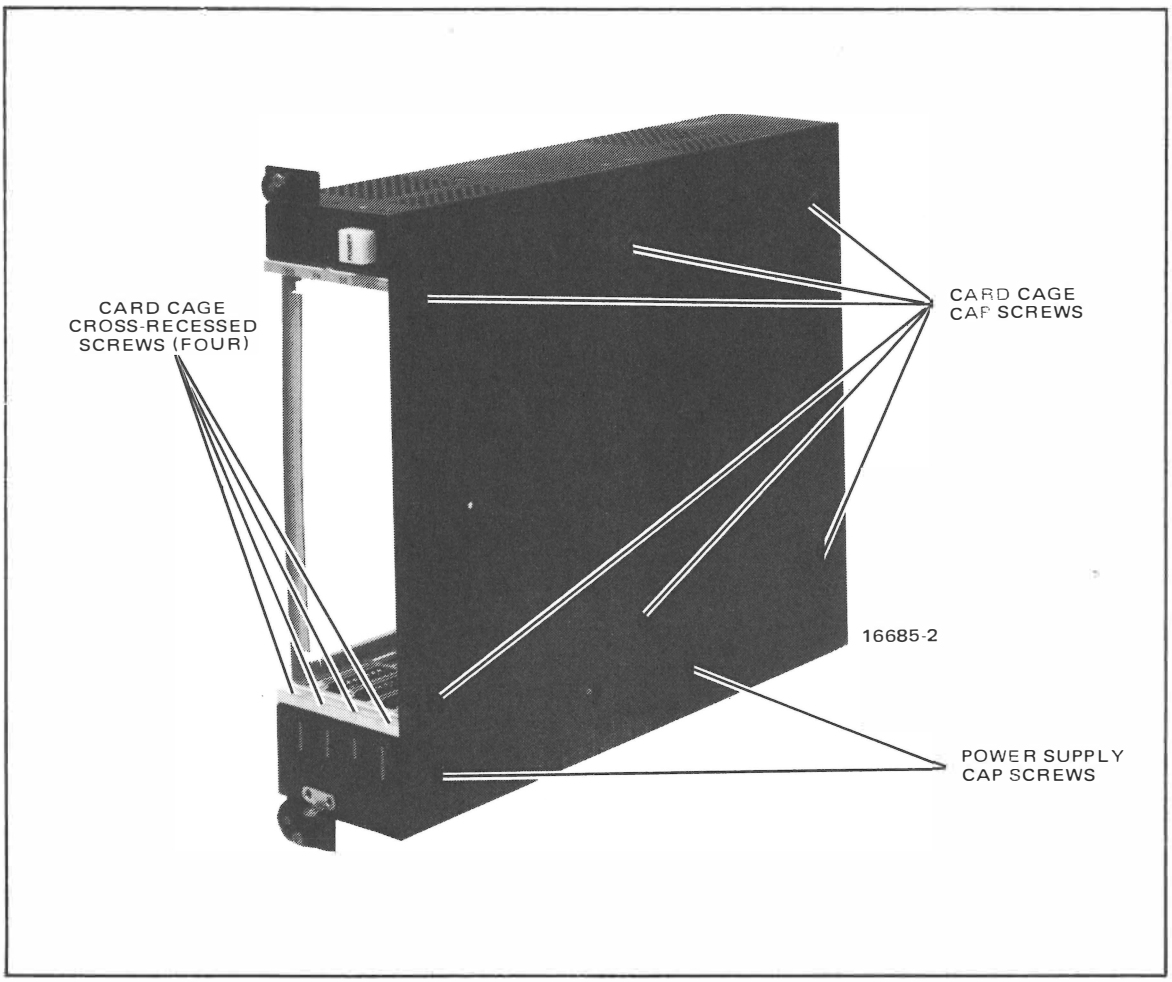


Figure 4-2. Card Cage and Power Supply Removal

STEP 4 Remove six capscrews which secure assembly to bottom of unit.

STEP 5 Slide assembly forward until motherboard connectors clear rear panel, then lift card cage assembly out of unit. Set assembly alongside the unit. (This can be done without disconnecting the harness as illustrated in Figure 4-3.)

Replace card cage assembly as follows:

STEP 6 Set assembly in unit and slide it back until motherboard connectors protrude through rear panel. Examine harness to make sure it is not pinched.

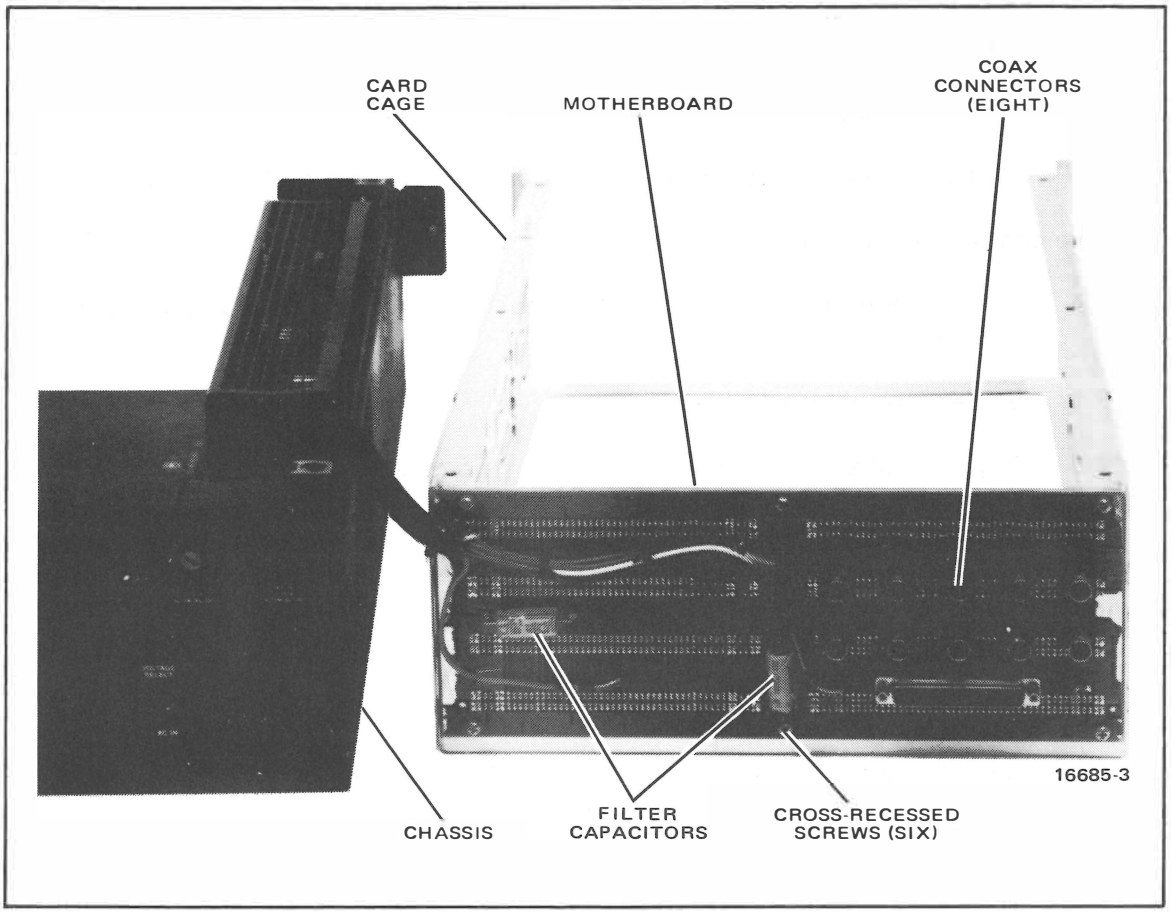


Figure 4-3. Card Cage Replaceable Components

STEP 7 Start two forward capscrews on bottom of unit.

STEP 8 Start four cross-recessed screws at front of assembly and then the remaining capscrews.

STEP 9 Install a PWA in bottom slot of card cage and tighten two bottom cross-recessed screws.

STEP 10 Install a PWA in top slot and tighten two top screws.

STEP 11 Tighten screws on bottom of unit.

STEP 12 Replace remaining PWAs. Verify that PWAs move freely in slots.

STEP 13 Close door, replace unit cover and tighten four quarter-turn latches.

4-4 Coaxial Connector

Remove coaxial connector as follows:

STEP 1 Remove card cage assembly as described in steps 1 through 5 of paragraph 4-3.

STEP 2 Unsolder two leads of connector to be removed.

STEP 3 Remove two connector retaining screws and remove connector.

Replace coaxial connector as follows:

STEP 4 Fasten replacement connector to motherboard with two retaining screws.

STEP 5 Solder two connector leads.

STEP 6 Replace card cage assembly in unit as described in steps 6 through 13 of paragraph 4-3.

4-5 Filter Capacitor

Remove filter capacitor as follows:

STEP 1 Remove card cage assembly from unit as described in steps 1 through 5 of paragraph 4-3.

STEP 2 Identify positive lead of capacitor to be replaced and identify feedthrough to which capacitor is connected.

STEP 3 Unsolder capacitor leads. If difficulty is experienced, cut leads near capacitor body.

Replace filter capacitor as follows:

STEP 4 Identify replacement capacitor positive lead.

STEP 5 If original capacitor was unsoldered, solder replacement normally, making sure positive lead is connected to correct feedthrough. If leads were cut, connect and solder replacement capacitor positive and negative leads to positive and negative cut leads.

STEP 6 Replace card cage assembly in unit as described in steps 6 through 13 of paragraph 4-3.

4-6 Motherboard Assembly

Remove motherboard assembly as follows

STEP 1 Remove card cage assembly from unit as described in steps 1 through 5 of paragraph 4-3.

STEP 2 Set chassis on its side to gain access to two capscrews which secure the power supply to chassis bottom. (Refer to Figure 4-2.)

STEP 3 Remove two screws and set power supply between chassis and cage. (See Figure 4-4.)

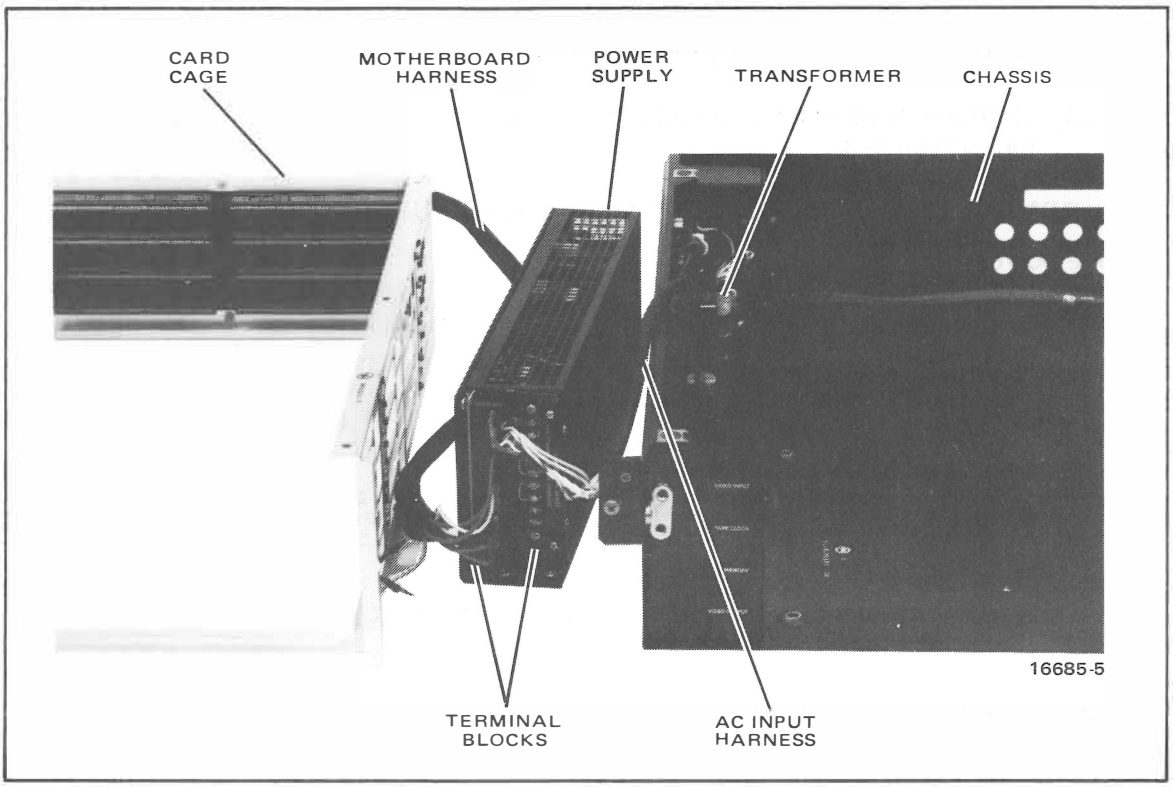


Figure 4-4. Motherboard and Power Supply Replacement

STEP 4 Record color code for harness wire or wires at each terminal of terminal block where motherboard harness is connected.

STEP 5 Disconnect motherboard harness.

STEP 6 Remove six cross-recessed screws securing motherboard assembly to card cage assembly and remove motherboard assembly.

Replace motherboard assembly as follows:

STEP 7 Start six screws that secure motherboard assembly to card cage assembly.

STEP 8 Install bottom and top PWAs in card cage assembly, making sure that edge connectors are firmly seated.

STEP 9 Tighten six screws and remove PWAs.

STEP 10 Connect motherboard harness to power supply. (Refer to color code list prepared in step 4.)

STEP 11 Place power supply in position in chassis with harnesses between power supply and chassis side.

STEP 12 Start two screws that secure power supply. Verify that harnesses will not be pinched and then tighten screws.

STEP 13 Replace card cage assembly in unit as described in steps 6 through 13 of paragraph 4-3.

4-7 REMOVING AND REPLACING THE POWER SUPPLY

Remove power supply as follows:

STEP 1 Remove card cage assembly as described in steps 1 through 5 of paragraph 4-3.

STEP 2 Set chassis on its side to gain access to two capscrews which secure power supply to chassis bottom. (See Figure 4-2.)

STEP 3 Remove two screws and set power supply between chassis and cage. (See Figure 4-4.)

STEP 4 Record color code for harness wire or wires at each terminal of the two terminal blocks.

STEP 5 Disconnect harnesses and remove power supply.

Replace power supply as follows:

STEP 6 Install sense jumpers on replacement power supply to match those on the power supply being replaced.

STEP 7 Connect harnesses to power supply. (Refer to color code list prepared in step 4.)

STEP 8 Place power supply in position in chassis with two harnesses between power supply and chassis side.

STEP 9 Start two capscrews that secure power supply. Verify that harnesses will not be pinched and then tighten screws.

STEP 10 Replace card cage assembly in chassis as described in steps 6 through 13 of paragraph 4-3.

4-8 REMOVING AND REPLACING THE POWER TRANSFORMER

Remove power transformer as follows:

STEP 1 Remove card cage assembly as described in steps 1 through 5 of paragraph 4-3 and set assembly alongside unit.

STEP 2 Remove power supply as described in steps 1 through 3 of paragraph 4-7.

Note

Observe arrangement of harnesses between transformer (Refer to Figure 4-4.) and rear corner of chassis. Before replacing transformer, these harnesses must be restored to their original position or difficulty will be experienced in positioning the transformer.

STEP 3 Record color code for harness wire at each terminal of transformer.

STEP 4 Disconnect transformer wires.

STEP 5 Remove two nuts securing transformer to chassis bottom.

STEP 6 Lift ground lug and transformer off transformer mounting studs.

Replace power transformer as follows:

STEP 7 Restore harnesses in corner of chassis to their original positions and place transformer in position on mounting studs.

STEP 8 Replace ground lug and run nuts on finger tight.

STEP 9 Verify that wiring will not be pinched by transformer and tighten nuts.

STEP 10 Reconnect transformer wires. Refer to color code list prepared in step 3.

STEP 11 Replace power supply as described in steps 8—10 of paragraph 4-7.

STEP 12 Replace card cage assembly in chassis as described in steps 6 through 13 of paragraph 4-3.

4-9 REMOVING AND REPLACING FAN UNITS

Remove fan units as follows:

STEP 1 Remove card cage assembly as described in steps 1 through 5 of paragraph 4-3.

STEP 2 Disconnect power connector from fan unit. (See Figure 4-5.)

STEP 3 Remove four hex-socket capscrews that secure fan unit to chassis and remove fan unit.

Replace fan unit as follows:

STEP 4 Secure replacement fan unit to chassis with four screws.

STEP 5 Reinstall power connector on fan unit.

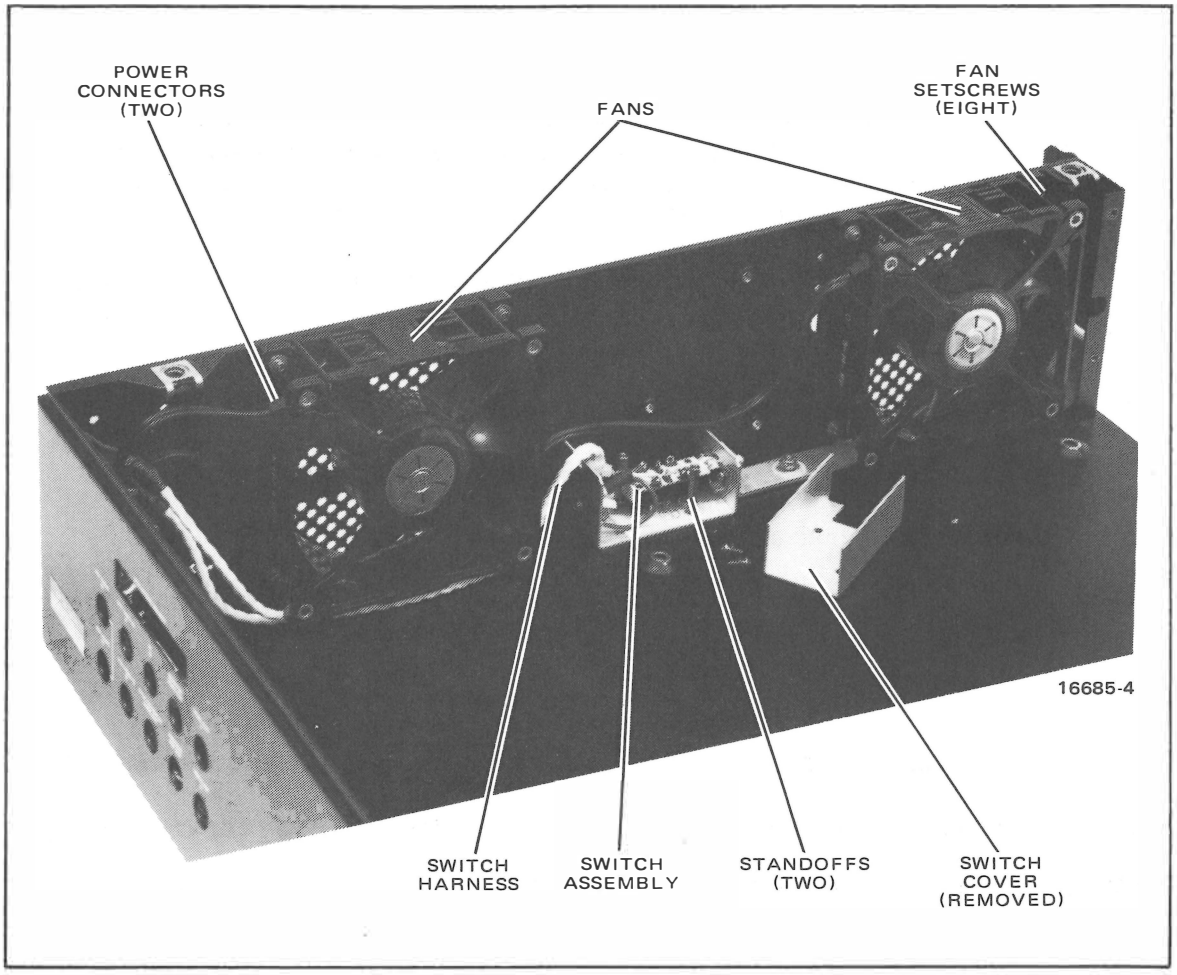


Figure 4-5. Fan Unit and Switch Assembly Replacement

STEP 6 Replace card cage assembly in chassis as described in steps 6 through 13 of paragraph 4-3.

4-10 REMOVING AND REPLACING AC POWER SWITCH ASSEMBLY

Remove ac power switch assembly as follows:

STEP 1 Remove card cage assembly as described in steps 1 through 5 of paragraph 4-3.

STEP 2 Remove two screws holding switch assembly cover and remove cover. (See Figure 4-5.)

STEP 3 Remove two standoffs. Lift switch assembly off studs and disconnect linkage.

STEP 4 Disconnect switch assembly harness from terminal block.

Replace ac power switch as follows:

STEP 5 Set switch assembly on mounting studs and connect linkage.

STEP 6 Replace standoffs finger tight.

STEP 7 Tighten standoff. Press and release POWER pushbutton to verify that linkage moves freely. If linkage sticks, loosen standoffs, shift switch assembly position, and repeat this step.

STEP 8 Replace switch assembly cover and two screws that secure it.

STEP 9 Reconnect switch assembly harness to terminal block.

STEP 10 Replace card cage assembly as described in steps 6 through 13 of paragraph 4-3.

SECTION 5
SUPPLEMENTAL INFORMATION

5-1 INTRODUCTION

This section contains detailed lists and drawings which supplement the maintenance information and procedures.

5-1 Selectable Jumper Options

Tables 5-1 through 5-4 are lists of individual jumpers and their recommended settings. If a problem is encountered during installation or after maintenance on any PWA, check jumper selection on individual assemblies. Jumper options should conform to normal settings of the jumper or to a specific option as required by the particular system configuration.

Table 5-1. Video Input PWA Jumper Locations

Jumper	Description	Position	Option
P1	2.5 MHz luma LPF	Removed A-B	Normal Factory test
P2	2.5 MHz luma LPF	Removed A-B	Normal Factory test
P3	2.5 MHz luma LPF	A-B Removed	Normal Factory test
P4	2.5 MHz luma LPF	A-B Removed	Normal Factory test
P5	2.5 MHz luma LPF	Removed A-B	Normal Factory test
P6	6 MHz LPF	Removed A-B	Normal Factory test
P7	6 MHz LPF	A-B Removed	Normal Factory test
P8	Burst locked oscillator	A-B Removed	Factory test Normal

(Continued next page)

Table 5-1. Video Input PWA Jumper Locations

Jumper	Description	Position	Option
P9	Search dropout range	A-B B-D B-C	On (normal) Off Factory test
P10	RF dropout	A-B B-C	Normal VPR-20
P11	Test ramp	A-B B-C	Normal Test ramp
P12	H-gate	A-B Removed	Normal Factory test
P14	Vertical	A-B B-C	Broad pulse (normal) Equalizing pulse (VPR-20 only)
P15	Dropout gate	A-B B-C	Off (normal) On
P16	Decode error	A-B A-C	Normal Factory test

Table 5-2. Tape Clock PWA Jumper Locations

Jumper	Description	Position	Option
P1	Search VCO up	A-B A-C	Normal Factory test
P2	Normal VCO	A-B A-C	Normal Factory test
P3	Search VCO down	A-B A-C	Normal Factory test
P4	Encode	A-B A-C	Normal Factory test
P5	Line error	A-B A-C	Normal Factory test

(Continued next page)

Table 5-2. Tape Clock PWA Jumper Locations

Jumper	Description	Position	Option
P6	25 Hz	A-B A-C	Normal Factory test
P7	Burst loop	A-B A-C	Normal Factory test
P8	Sync terminate	A-B A-C A-D A-E	Auto (normal) On Off Up
P9	Burst/sync ramp	A-B Removed	Normal Factory test
P10	X2 disable	A-B A-C	Normal Off
P11	+90°	A-B A-C	Normal Factory test
P12	Line-by-line correction	A-B A-C	Normal Factory test
P13	-90°	A-B A-C	Normal Factory test
P14	Vel comp process	A-B A-C	Normal Factory test
P15	Edit ready	A-B A-C	360° 180°
P16	Sync head	A-B A-C	Off (Normal) Auto
P17	Edit ready inhibit	A-B A-C	Normal Factory test
P18	Vertical dropout	A-B A-C	Normal Wide (Het)
P19	Inhibit	A-B A-C	Normal Factory test

(Continued next page)

Table 5-2. Tape Clock PWA Jumper Locations (Continued)

Jumper	Description	Position	Option
P20	Tape vertical	A-B A-C	Normal Factory test
P21	Color present	A-B A-C	Normal Factory test
P22	Vertical noise	A-B A-C	Normal Low
P23	7.8 kHz reset	A-B A-C	On (normal) Off
P24	Write vertical processor	A-B A-C	On (normal) Off
P25	Qualify	A-B A-C	Normal Factory test
P26	Write Delay	A-B A-C	Normal Factory test
P27	Playback vertical	A-B A-C	Normal Factory test
P28	Normal VCO disable	A-B A-C	Normal Factory test
P29	Reset enable	A-B A-C	Normal Factory test
P30	VCO mode	A-B A-C A-D	Auto Search LC (het)

Table 5-3. Memory system PWA Jumper Locations

Jumper	Description	Position	Option
P1	Read 4Fsc feedback	A-B Removed	Normal Factory test

(Continued next page)

Table 5-3. Memory System PWA Jumper Locations (Continued)

Jumper	Description	Position	Option
P2	Read 4Fsc output	A-B Removed	Normal Factory test
P3	Read 4Fsc oscillator	A-B A-C	Normal Factory test
P4	Quadrant offsets	A-B A-C	Normal Factory test
P5	Line-by-line error	A-B A-C A-D	Normal Factory test Factory test
P6	Velocity compensator	A-B A-C	On (normal) Off
P7	Line error gain	A-B A-C	Normal Factory test
P8	V-axis disable	A-B A-C	Normal Factory test
P9	Write process logic	A-B A-C	Normal Disable A
P10	Overload mode	A-B A-C	Normal Soft
P11	Rewrite	A-B A-C	Normal Disable RW
P12	Dual write	A-B A-C	Normal Disable DW
P13	Memory centering	A-B A-C	Vertical (normal) Memory
P14	Write vertical processing	A-B A-C	On (normal) Off
P15	Slo-mo center	A-B A-C	On (normal) Off

Table 5-4. Video Output PWA Jumper Locations

Jumper	Description	Position	Option
P1	EBU/variable sync/ burst	A-B A-C	EBU Variable
P2	Output clamp	A-B B-C	Normal Factory test
P3	Input clamp	A-B A-C	Normal Factory test
P4	Advanced reference level	A-B A-C	-4V level Video level
P5	Sine X/X	A-B Removed	Factory test Normal
P6	Sine X/X	A-B Removed	Factory test Normal
P7	LPF	A-B Removed	Factory test Normal
P8	Chroma gain	A-B A-C	Normal Factory test
P9	Black clip clamp	A-B A-C	Normal Factory test
P10	Video out	A-B A-C	Normal Factory test
P11	Sine X/X	A-B Removed	Normal Factory test
P12	Video out 2 sync	A-B A-C	On Off
P13	Sine X/X	A-B Removed	Normal Factory test
P14	D/A output	A-B A-C	Normal Factory test
P15	Advanced reference	A-B A-C	Composite sync Vertical drive
P16	Sync blank	A-B Removed	Normal Factory test
P17	Reference 4Fsc	A-B Removed	Normal Factory test

5-3 Test Points

Tables 5-5 through 5-8 list test points located on each PWA and give a brief description of the signal at the test point.

Table 5-5. Video Input PWA Test Points

Test Point	Description	Test Point	Description
1	Luminance LPF output	32	Tape horizontal.(–)
2	Filter video output	33	H-gate control
3	Video path 6-MHz LPF output	34	Normal/search
4	A/D clamped video	35	Burst present pulse (–)
5	A/D reference – 2.00V	36	Video mute (–)
6	Tape video input B	37	Gated sync (–)
7	Tape video input A	38	Up/down
8	Monitor video output	39	Wide/narrow
9	Digital burst to Tape Clock PWA	41	Back porch sample voltage (50% slicer)
10	Video A/B selector switch output		
11	Normal video output	42	50% sync slicer voltage
12	V-axis	43	VPR dropout (–)
13	Test ramp generator	44	50% point sliced composite sync (–)
14	U-axis		
17	Burst filter output	45	RF dropout (–)
18	A/D feedback clamp voltage	46	Color processor (–)
19	Decoded R-Y signal	47	Normal heterodyne (+)
20	Sync coherent subcarrier output	48	RF dropout input (after amplifier/buffer stage)
21	A/D clamp		
24	Velocity compensator write pulse (-)	49	RF dropout (AM detector output)
		50	Chroma BPF output
25	Crude sync slicer level	51	Chroma demodulator clamp voltage
26	Crude slicer sync output		
27	Composite dropout (–)	52	Burst locked oscillator error voltage
28	Color processor clamp		
29	Noise gate sync (–)	58	+12 VA
30	Burst gate (+)	59	-12 VA
31	Sample inhibit (+)	60	+5 VD

Table 5-6. Tape Clock PWA Test Points

Test Point	Description	Test Point	Description
1	Normal VCO error voltage	3	A-ground
2	+12 VA	4	– 12 VA

(Continued next page)

Table 5-6. Tape Clock PWA Test Points (Continued)

Test Point	Description	Test Point	Description
5	Tape 2Fsc	27	D-ground
6	Analog frequency error	28	−5.2V
7	+12VA	29	A-ground
8	A-ground	30	A-ground
9	−12 VA	31	A-ground
10	Normal 4Fsc	32	D-ground
12	−5 VA	33	D-ground
13	25 Hz mod H-sync	34	D-ground
14	Burst/sync ramp	35	D-ground
15	−12 VA	36	D-ground
16	A-ground	37	D-ground
17	+12 VA	38	D-ground
18	Comparator timing (H-coherent burst crossing)	39	D-ground
		40	Phase-lock loop pulse
19	Digital burst	41	VCO and comp range
20	D-ground	42	Decode vector comp
21	+5 VD	43	Line error and sample
22	Tape 4 Fsc	44	Burst/sync comparator bias
23	Tape 4Fsc	45	H-delay output
24	+5 VD	46	Burst sync phase
25	D-ground	47	25 Hz mod H-sync
26	+5 VD	48	Quadrature select

Table 5-7. Memory System PWA Test Points

Test Point	Description	Test Point	Description
1	Read 4Fsc oscillator error voltage	5	−12 VA
2	+12 VA	6	Cycle clock generator output
3	Next line time base error and quadrant error	7	Start Read
		8	+5 VD
4	Time-base error within 90°		

Table 5-8. Video Output PWA Test Points

Test Point	Description	Test Point	Description
1	Input sync	32	Chroma gain stage input
2	Phase comp input	33	Video D/A converter output
3	Ref input amp output	34	H-2Fsc
4	Ref input amp	35	H-4Fsc
5	Sync stripper output	39	Subcarrier output-to-burst adder
6	Reference video low-pass filter output	40	−5.2 VD
		41	Sine V/2
7	Sync stripper input	43	Read pulse generator output
8	Reference video input	44	Divide-by-five clock
9	Error voltage to 4Fsc LC oscillator	45	Ref comp sync
		46	B-Y input
10	Error voltage to 4Fsc crystal oscillator	47	R-Y input
		48	Ref H-counting
11	Ref 4Fsc	49	Comp blanking
14	Filtered video	50	H-blanking
15	Noncomposite clamped video	51	Ref H-counting
16	Burst Fsc	52	V/32 counting circuit
17	Advance reference output	53	Chroma subcarrier
20	Burst present	54	Hz Fsc
21	Ref 2Fsc	55	−12 VD
22	Subcarrier phase	56	RF supply
25	Video chroma gain stage output	57	V/2
26	Low-pass filter and sin x/x equalizer output	58	Bit 2
		59	Bit 3
27	−12 VA	60	V/32 counting circuit
28	+12 VA	61	V/32 counting circuit
29	Ref 7.8 kHz	62	V/32 counting circuit
30	V/2 reset	63	Step left
31	Ref present	64	+5 VD

5-4 TBC-6 Motherboard PWA

Table 5-9 is a list of TBC-6 Motherboard PWA signals and their descriptions.

Table 5-9. Motherboard PWA Signal Pinouts

Pin	Signal	Source/PWA
1	Analog Ground	Power Supply
2	Analog Ground	Power Supply
3	Analog Ground	Power Supply

(Continued next page)

Table 5-9. Motherboard PWA Signal Pinouts (Continued)

Pin	Signal	Source/PWA
4	Analog Ground	Power Supply
5	+12 Vdc	Power Supply
6	+12 Vdc	Power Supply
7	+12 Vdc	Power Supply
8	+12 Vdc	Power Supply
9	Analog Ground	Power Supply
10	Analog Ground	Power Supply
11	Analog Ground	Power Supply
12	Analog Ground	Power Supply
13	Ref Video Input	J2 and J3 Ref Video
14	Ref Video Input	J2 and J3 Ref Video
15	Video Ground	J2 and J3 Ref Video
16	Video Ground	J2 and J3 Ref Video
17	Burst	Video Input
18	Burst	Video Input
19	Analog Ground	Video Output
20	Analog Ground	Video Output
21	Aux Video	Video Output
22	Aux Video	Video Output
23	Video Ground	J5 Tape Video Input B
24	Video Ground	J5 Tape Video Input B
25	Tape Video Input	J5 Tape Video Input B
26	Tape Video Input	J5 Tape Video Input B
27	Analog Ground	Power Supply
28	Analog Ground	Power Supply
29	Video Ground	J4 Tape Video Input A
30	Video Ground	J4 Tape Video Input A
31	Tape Video Input	J4 Tape Video Input A
32	Tape Video Input	J4 tape Video Input A
33	Analog Ground	Power Supply
34	Analog Ground	Power Supply
35	Sync Coherent Subc Output	Video Input
36	Sync Coherent Subc Output	Video Input (to J7 sync coherent
37	Analog Ground	Video Input subc out)
38	Analog Ground	Video Input
39	RF Input	J6 RF Input
40	RF Input	J6 RF Input
41	RF Ground	J6 RF Input
42	RF Ground	J6 RF Input
43	Analog Ground	Power Supply
44	Analog Ground	Power Supply
45	Step Forward 2	J1-32 (VTR)

(Continued next page)

Table 5-9. Motherboard PWA Signal Pinouts (Continued)

Pin	Signal	Source/PWA
46	Step Forward 1	J1-31
47	Sync HD Processor	J1-30
48	Up/Down	J1-12
49	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14–19
50	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14–19
51	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14–19
52	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14–19
53	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14–19
54	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14–19
55	2H Gate	J1-28
56	Dropout Pulse	J1-29
57	Slow Motion	J1-27
58	Zero Offset	J1-9
59	HD Sw/Vertical Dropout	J1-25
60	P/B Vertical	J1-26
61	Tachometer	J1-24
62	Fast Shuttle	J1-6
63	Sync Retard	J1-23
64	Edit Mute	J1-5
65	Step Back 1	J1-20
66	Step Back 2	J1-21 (VTR)
67	Analog Ground	Video Output } (to J9 adv rev)
68	Analog Ground	Video Output
69	Advance Sync Output	Video Output
70	Advance Sync Output	Video Output
71	Video Ground	Video Input } (to J8 monitor video)
72	Video Ground	Video Input
73	Monitor Video Output	Video Input
74	Monitor Video Output	Video Input
75	Analog Ground	Power Supply
76	Analog Ground	Power Supply
77	Video Output II	Video Output } (to J11 video output II)
78	Video Output II	Video Output
79	Video Ground	Video Output
80	Video Ground	Video Output } (to J10 video output I)
81	Video Output I	Video Output
82	Video Output I	Video Output
83	Video Ground	Video Output
84	Video Ground	Video Output
85	Analog Ground	Power Supply
86	Analog Ground	Power Supply
87	−5 Vdc	Power Supply

(Continued next page)

Table 5-9. Motherboard PWA Signal Pinouts (Continued)

Pin	Signal	Source/PWA
88	– 5 Vdc	Power Supply
89	Analog Ground	Power Supply
90	Analog Ground	Power Supply
91	Analog Ground	Power Supply
92	Analog Ground	Power Supply
93	– 12 Vdc	Power Supply
94	– 12 Vdc	Power Supply
95	– 12 Vdc	Power Supply
96	– 12 Vdc	Power Supply
97	Analog Ground	Power Supply
98	Analog Ground	Power Supply
99	Analog Ground	Power Supply
100	Analog Ground	Power Supply
101	Digital Ground	Power Supply
102	Digital Ground	Power Supply
103	Digital Ground	Power Supply
104	Digital Ground	Power Supply
105	+ 5 Vdc	Power Supply
106	+ 5 Vdc	Power Supply
107	+ 5 Vdc	Power Supply
108	+ 5 Vdc	Power Supply
109	Digital Ground	Power Supply
110	Digital Ground	Power Supply
111	Digital Ground	Power Supply
112	Digital Ground	Power Supply
113	Read 4Fsc	Memory
114	Read 4Fsc	Memory
115	DO8	Memory
116	DO7	Memory
117	DO6	Memory
118	DO5	Memory
119	DO4	Memory
120	DO3	Memory
121	DO2	Memory
122	DO1	Memory
123	Digital Ground	Power Supply
124	Digital Ground	Power Supply
125	Reference 4Fsc	Video Output
126	Reference 4Fsc	Video Output
127	Reference H (-)	Video Output
128	Reference 7.8 kHz (H/2)	Video Output
129	Reference V (+)	Video Output

(Continued next page)

Table 5-9. Motherboard PWA Signal Pinouts (Continued)

Pin	Signal	Source/PWA
130	Reference V/2	Video Output
131	Reference V/4	Video Output
132	Reference Comp. Sync (–)	Video Output
133	Ref 3.9 kHz (H/4)	Tape Clock
134	Read Pulse	Tape Clock
135	Sync Terminate (–)	Video Input
136	Wide (-)	Video Input
137	Normal (+)/Heterdoyne (–)	Memory
138	Normal (+)/Bypass (–)	Memory
139	Video Input Switch	Memory
140	DOC Off (–)	Memory
141	Color Present (+)	Video Input
142	VCO Lock (–)	Tape Clock
143	Search (–)	Tape Clock
144	VCO Up (-)/Down (+)	Video Input
145	Video Mute (–)	Video Input
146	Gen Lock (–)	Video Output
147	Color Shuttle Limit (–)	Video Input
148	Digital Burst	Video Input
149	No Connection	
150	No Connection	
151	No Connection	
152	No Connection	
153	No Connection	
154	No Connection	
155	Digital Ground	Power Supply
156	Decode Fsc	Tape Clock
157	Gated DO (–)	Tape Clock
158	Vertical Inhibit (–)	Tape Clock
159	VCO Vertical	Tape Clock
160	F/2	Memory
161	Tape V/2	Tape Clock
162	Tape Vertical	Video Input
163	Burst Present (–)	Video Input
164	Tape H (–)	Video Input
165	Heterodyne 7.8 kHz	Tape Clock
166	Write 7.8 kHz	Memory
167	Write 3.9 kHz	Memory
168	1/2 Line (–)	Tape Clock
169	Clamp Pulse (–)	Tape Clock
170	Flywheel Sync (–)	Tape Clock
171	Gated Sync	Video Input
172	Vel Comp Write (–)	Memory

(Continued next page)

Table 5-9. Motherboard PWA Signal Pinouts (Continued)

Pin	Signal	Source/PWA	
173	VCO Write Timing (–)	Tape Clock	
174	Write Pulse (–)	Tape Clock	
175	Encode Fsc	Tape Clock	
176	Encode Fsc	Tape Clock	
177	Digital Ground	Power Supply	
178	Digital Ground	Power Supply	
179	D18	Video Input + Tape Clock	Pull up on Memory System PWA
180	D17	Video Input + Tape Clock	
181	D16	Video Input + Tape Clock	
182	D15	Video Input + Tape Clock	
183	D14	Video Input + Tape Clock	
184	D13	Video Input + Tape Clock	
185	D12	Video Input + Tape Clock	
186	D11	Video Input + Tape Clock	
187	Tape 4Fsc	Tape Clock	
188	Tape 4Fsc	Tape Clock	
189	Digital Ground	Power Supply	
190	Digital Ground	Power Supply	
191	Digital Ground	Power Supply	
192	Digital Ground	Power Supply	
193	+5 Vdc	Power Supply	
194	+5 Vdc	Power Supply	
195	+5 Vdc	Power Supply	
196	+5 Vdc	Power Supply	
197	Digital Ground	Power Supply	
198	Digital Ground	Power Supply	
199	Digital Ground	Power Supply	
200	Digital Ground	Power supply	

5-5 Adjustments

Tables 5-10 through 5-13 list the adjustment reference designations and their functions.

Table 5-10. Video Input PWA Adjustments

Reference Designation	Function
L1	Color processor LPF filter adjustment
L2	Color processor LPF filter adjustment

(Continued next page)

Table 5-10. Video Input PWA Adjustments (Continued)

Reference Designation	Function
L6	6 MHz LPF adjustment
L7	6-MHz LPF adjustment
L10	Color processor LPF filter adjustment
L11	Color processor LPF filter adjustment
L12	Color processor chroma inverter peaking coil
L14	Color processor chroma BPF adjustment
L17	Color processor chroma BPF adjustment
L18	Color processor burst oscillator LPF
L22	Color processor burst oscillator LPF
L23	Color processor burst locked oscillator adjustment
L25	Burst filter adjustment
L26	Burst filter adjustment
R11	Color processor luminance gain
R123	Monitor video output amplifier gain
R126	Color processor B-Y demodulator gain balance.
R127	Color processor B-Y demodulator dc balance
R136	Color processor heterodyne chroma gain.
R142	Color processor chroma inverter dc balance
R158	A/D high frequency response
R165	A/D reference adjustment for −2.00V at TP15
R213	A/D clamp level adjustment
R219	Color processor modulator phase balance
R280	Video input unity gain calibrate
R297	Color processor R-Y demodulator dc balance
R298	Color processor burst locked oscillator error offset
R345	Color processor heterodyne chroma phase
R346	Sync separator servo loop adjustment. Set midrange
R347	Sync separator servo loop adjustment 8.00V at TP39
R373	Second vertical equalizer delay adjustment
R401	Slow motion sync delay
R426	Dropout stretch adjustment
R441	RF dropout adjustment
R449	RF dropout AGC level
R467	RF dropout adjustment
R469	Color processor chroma inverter gain

(Continued next page)

Table 5-10. Video Input PWA Adjustments (Continued)

Reference Designation	Function
R470	Color processor chroma inverter balance
R472	Front panel video input level
T1	Color processor LPF adjustment
T2	Color processor LPF adjustment
T3	6 MHz LPF adjustment
T4	Color processor delay equalizer adjustment

Table 5-11. Tape Clock PWA Adjustments

Reference Designation	Function
C8	Search UP oscillator frequency
C196	Search DOWN oscillator frequency
L1	Frequency discriminator adjustment
L2	Normal VCO frequency adjustment
R39	Test of search VCO oscillator range (with J2, J3)
R63	DOWN search oscillator error gain
R68	UP search oscillator error gain
R75	Burst/VCO ramp offset
R79	Burst/VCO ramp gain
R101	Slow-motion static phase (edit ready)
R110	Analog frequency error dc offset
R111	Slow-motion vector compensation
R112	Slow-motion dynamic phase (edit ready)
R127	Permits test of DAC U39 (using J6)
R142	Test burst crossing loop error (with J7)
R158	Normal sync-burst phase (edit ready). CALIBRATE
R193	Horizontal phase (monochrome signal timing)
R195	Burst crossing timing
R198	Horizontal delay
R201	Horizontally coherent burst crossing adjust
R222	Heterodyne vertical dropout duration delay
R223	Heterodyne sync-burst phase
R224	Phase comparator center
R238	Normal VCO phase comparator range
R240	Tape-H reset qualify delay

Table 5-12. Memory System PWA Adjustments

Reference Designation	Function
L1	Read 4Fsc oscillator frequency
R15	DC offset, 4Fsc oscillator error
R28	Quadrature error adjust
R29	Quadrature error adjust
R39	Velocity compensator balance
R48	Velocity compensator gain (best blue vector).
R58	Line error test (see J4)
R59	Line error gain
R60	Offset (no velocity error in E-E)

Table 5-13. Video Output PWA Adjustments

Reference Designation	Function
L3	TBC video low pass filter setup
L4	TBC video low pass filter setup
L5	TBC video low pass filter setup
L7	Black clip differential phase
L8	TBC video low pass filter setup
L9	TBC video low pass filter setup
L11	Chroma phase adjust for TBC video chroma amplitude circuit
L12	Sync generator 4Fsc LC oscillator frequency
L13	Sync generator 4Fsc crystal oscillator frequency
R1	Sync generator monochrome reference delay
R30	TBC video blanking transition null
R46	TBC video output burst level
R95	TBC video output dc level
R102	TBC video output burst symmetry around blanking
R117	Output horizontal blanking leading edge timing
R118	Output horizontal blanking trailing edge timing
R119	Sync generator reference video input nonstandard sync/burst phase adjust (J3)
R129	TBC video output blanking timing
R144	TBC video black clip level

(Continued next page)

Table 5-13. Video Output PWA Adjustments (Continued)

Reference Designation	Function
R179	Sync generator input reference video RS170A sync/burst phase adjustment
R181	Sync generator burst crossing strobe phase balance
R202	TBC video black clip differential gain
R214	TBC video output sync level
R299	TBC video output unity gain preset
R300	Front panel TBC video output video level control
R301	Front panel TBC video output subcarrier phase
R302	RS170A LED center
R305	Sync generator burst crossing strobe timing
R345	Front panel black level adjustment
R347	RS170A LED tolerance
R359	Black level unity preset
R360	Chroma level unity preset
R361	Front panel chroma level
R365	Subcarrier symmetry adjustment
R391	Front panel chroma phase
R399	Chroma phase range
R422	Sync generator oscillator phase comparator input 1/2-line adjust
R426	Horizontal sync width
R428	RS170A output sync/burst phase (J12 A-B)
R437	Output burst phase (with S4)
R438	Nonstandard sync/burst phase range adjustment
R439	Nonstandard sync/burst phase (J12 B-C)
R443	Sync generator advance reference output sync/burst phase
R481	TBC video clamp pulse delay
R483	TBC video output burst flag delay
T1	TBC video low pass filter adjustment

SECTION 6
COMPONENT LOCATIONS

6-1 INTRODUCTION

This section contains jumper and component location drawings of the four TBC-6 PAL printed wiring assemblies.

6-2 Component Locations

Figures 6-1 through 6-4 illustrate the location of the individual jumpers on each PWA. To find the use of any particular jumper, refer to the tables in section 5. If a problem is encountered during installation or after maintenance on any PWA, check jumper selection on individual assemblies. Jumper options should conform to normal settings of the jumper or to a specific option as required by the particular system configuration.

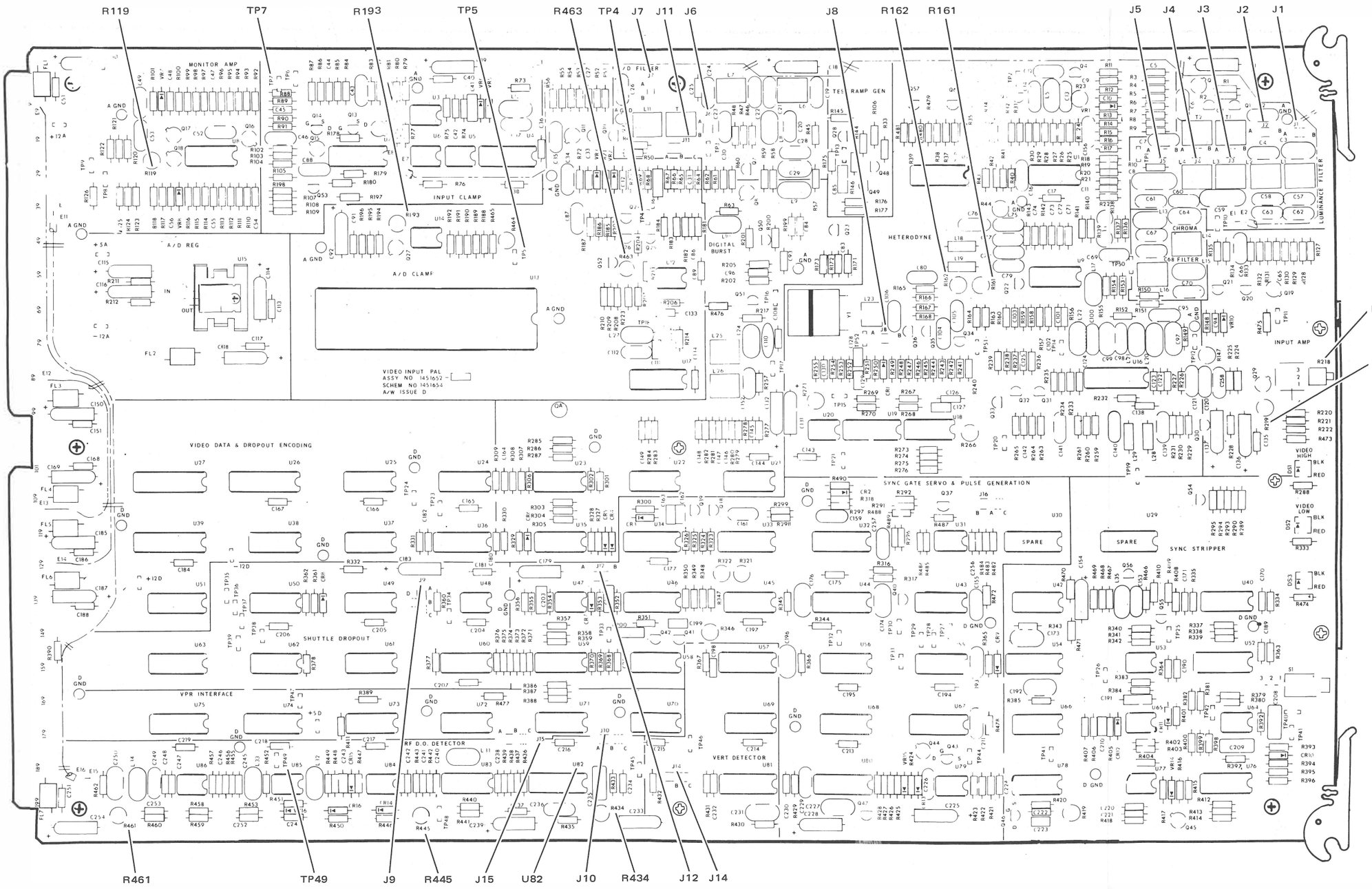


Figure 6-
TBC-6 Video Input PW
Component Locatio

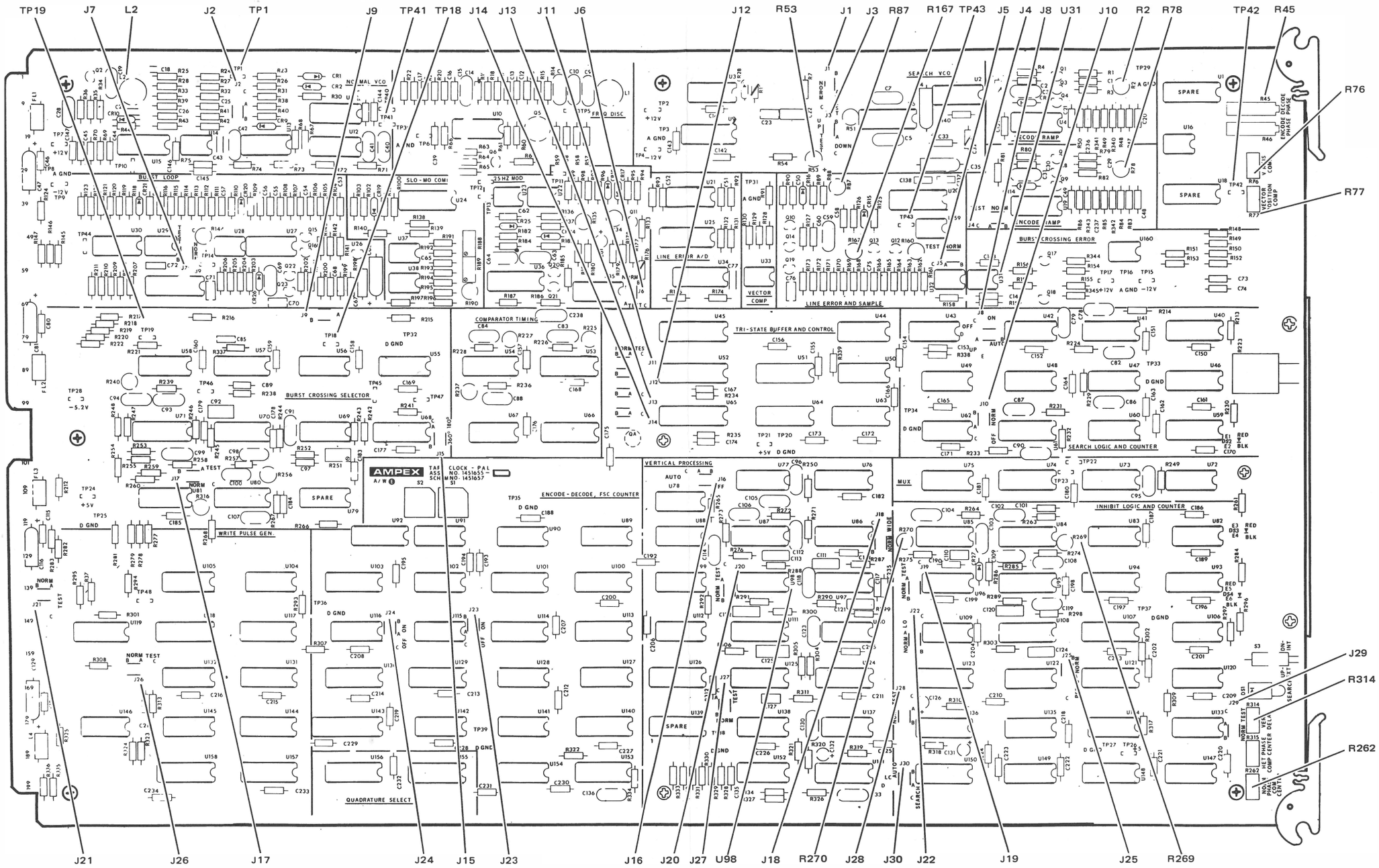


Figure 6-2.
TBC-6. Tape Clock PWA, Component Locations

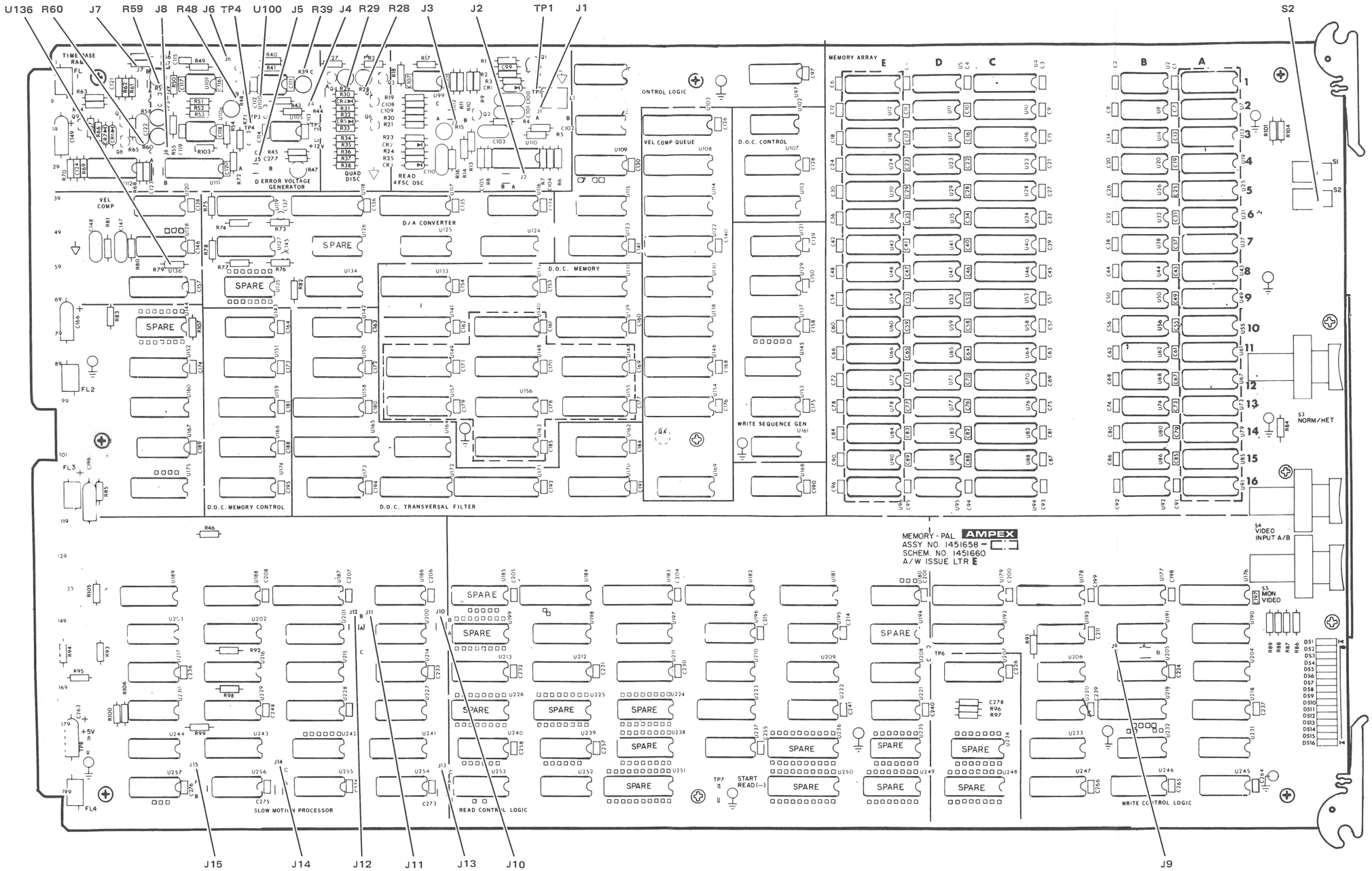


Figure 6
TBC-6 Memory System PW
Component Locatic

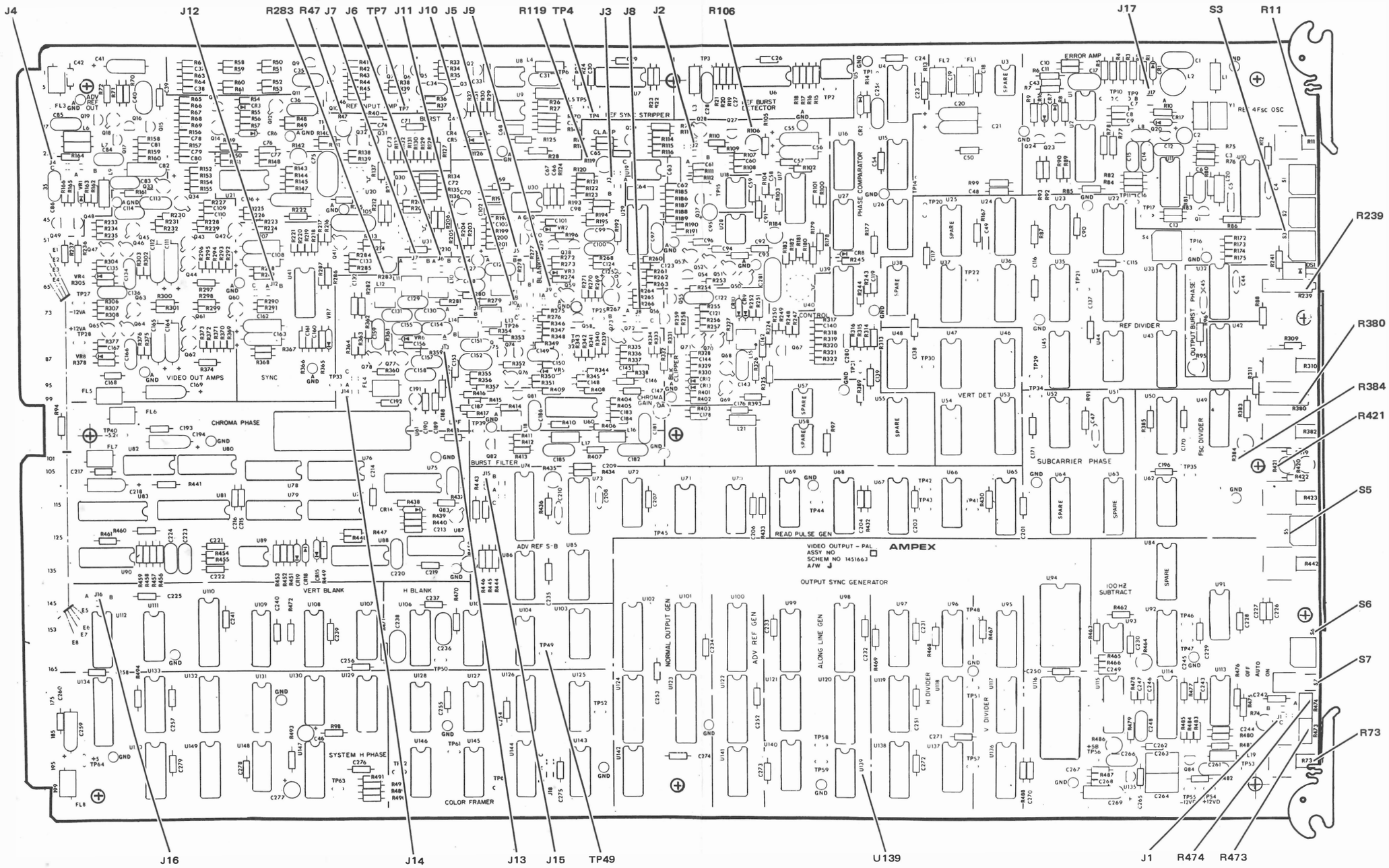


Figure 6-4.
TBC-6 Video Output PWA, Component Locations

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